5720 QUADRALOC DRIVE SYNCHRONISATION UNIT

PRODUCT MANUAL

HA058183

Issue 8

WARNING

NEVER WORK ON THE CONTROLLER
WITHOUT FIRST ISOLATING ALL
SUPPLIES TO THE SYSTEM.

TABLE OF CONTENTS

1 INTRODUCTION

The 5720 QUADRALOC shaft synchronisation product range is powered by 24V d.c. Supported by the 5702 range of products, the Eurotherm Drives microtach and the 5721 operator station, the 5720 provides the user with a complete solution to shaft synchronisation problems. The optional 5721 operator station and the RS422 serial link allow the user complete access and control of the 5720 operating parameters whilst ensuring an easy to use operator interface.

All control parameters within the 5720 are accessible via either the host serial link (RS422) or the operator station (5721). The operator station allows parameters to be scaled and ranged, which combined with user definable mesages and units allow the operator to enter data in meaningful engineering units. Similarly all system messages are displayed in meaningful words on a two line, sixteen character LCD display. Certain control parameters are connected to digital inputs, allowing the user to operate the 5720 in a stand-alone mode once configured.

Operation of the 5720 is based upon pre-configured software blocks. A number of these blocks are combined or configured to form a mode. Different combinations of blocks form different modes of operation, the mode of operation being selected via the host serial link, the operator station, or the digital inputs. Modes currently supported are speed lock, phase lock and register lock. In the speed lock mode the steady state speed of the reference and slave shafts are made equal by the 5720. The accuracy of speed lock is absolute and a ratio may be set between the shaft speeds with the range 0 ± 1.999999. Phase lock enables the relative positions of the two shafts to be controlled. Again accuracy is absolute whilst the same ratio range is provided along with a jog or inch facility. Register lock also allows the position of the reference and slave shafts to be controlled, as in phase lock, but the position of the two shafts may be locked at an absolute location by the use of reference and slave marks. These marks may be derived either from the 5701 Microtach or from an external source.

The drive interface is via analog setpoint and trim values. Positional data is obtained by optical incremental shaft encoders mounted (usually) on the reference and slave motors. The encoders used with the 5720 are the Eurotherm Drives Microtach (5701). These are conventional incremental encoders using a single fibre optic cable for data transmission. The use of fibre optic cable allows simple installation and a zero error rate when compared to conventional encoder units. The error free data transmission of Microtach combined with the high accuracy software of the 5720 provide the user with the most secure and accurate means of shaft synchronisation.

2 TECHNICAL DETAILS

2.1 GENERAL

Control action:	Fully digital Multiple modes each with a fixed block diagram Fixed point 64 bit number format with six decades of decimal resolution for high accuracy Full control of all parameters via RS422 serial link or user congifurable operator station (5721)
Looptime:	12mS. (Version 2.0 and 2.1) 15mS. (Version 2.2) 16mS. (Versions 2.3 to 2.11)
Speed/ position inputs:	By Eurotherm Drives fibre optic Microtach incremental encoder
Position register input:	By Eurotherm Drives Microtach By Fibre optic isolated external inputs
Steady state accuracy:	Absolute. (0.0% error)
Parameter resolution:	0.000001. (0.0001%)
Drive connection:	By analog voltages
Diagnostics:	Fully computerised with first fault latch Diagnostic monitoring via RS422 serial link or 5721 operator station LED diagnostic indicators on board
5721 operator station:	Full access to all parameters & variables via a security password Fully user configurable operator display using a two line by sixteen character LCD display User definable names for parameters & variables User definable names for engineering units All operator selectible parameters and variables may be scaled and ranged for the operator display

2.2 ELECTRICAL RATINGS

Power supply:	+24V ± 4V dc at 450mA [700mA with 5721 Op-Stn and two 5701 Microtachs] Allowance should be made for any additional units being supplied from the 5720. (Eg: 5702 and Microtach)
Maximum encoder frequency A, B:	57.6kHz. [5701]
Maximum encoder rotational speed:	3000 RPM. (1000 line/rev = 50 kHz). [5701]
Ambient temperature range:	0 to 55°C
Storage Temperature:	- 20°C - + 70°C short term (100 hours) 0°C - + 55°C long term Protect from direct sunlight. Ensure dry, corrosive free environment.

2.3 MECHANICAL DETAILS

Mounting centres:	Vertical - 255mm (10.04") Horizontal- 37.5mm (1.48") M6 fixing
Overall width:	75mm. (2.95")
Overall height:	275mm. (10.83")
Overall depth:	220mm. (8.66")
Weight:	1.7Kg. (3.75lbs)
Cable terminations:	Plug-in terminal blocks with retaining clips
Fibre terminations:	Push in fibre optic connectors
Access:	By removable lift-off cover

3 PRODUCT CODE

The QUADRALOC synchronisation system is identified by a 26 digit product code. All versions of the QUADRALOC family are known by the generic product number of 5720. The product code is constructed from seven blocks, as listed below.

Block No	No. of digits	Function
1	4	Basic product code.
2	2	Hardware build option.
3	3	Software build option.
4	2	Hardware special option.
5	7	Reference external marker source. Reference encoder message rate. Feedback external marker source. Feedback encoder message rate. Analog trim 100% or 10% strength.
6	4	Reference encoder resolution.
7	4	Feedback encoder resolution.

BLOCK 1 Four digits identifying the basic product.
5720 24V d.c. Powered QUADRALOC synchronisation unit.

BLOCK 2 Two digit code which specifies the build option of the unit.

Default is 00 (Standard build)

BLOCK 3 Three digit code defining the software build option.
Default is 000. (Standard software).

BLOCK 4 Hardware special option.
2 digit code defining hardware special options.
Default is 00 (Standard hardware).

BLOCK 5 Seven digit code defining the position of the hardware jumpers.

First digit defines the source of the external marker.(J1).
0 Reference MEXT is the external marker.
1 Reference MEXT is the encoder marker.
Default is 0.

Second digit defines the reference encoder message rate.(J2).
0 Encoder message rate is low speed. (460.8kHz).
1 Encoder message rate is high speed. (921.6kHz).
Default is 0.

Third digit defines the source of the external marker.(J3).
0 Feedback MEXT is the external marker.
1 Feedback MEXT is the encoder marker.
Default is 0.

Fourth digit defines the feedback encoder message rate.(J4).
0 Encoder message rate is low speed. (460.8kHz).
1 Encoder message rate is high speed. (921.6kHz).
Default is 0.

Fifth digit defines the analog trim maximum gain.(J5).
0 Analog trim 10%.
1 Analog trim 100%.
Default is 0.

Sixth and seventh digits are reserved for future use. Default for each is 0.

BLOCK 6 Four digit code specifying the reference encoder resolution.
Default is 1000 lines/rev.

BLOCK 7 Four digit code specifying the feedback encoder resolution.
Default is 1000 lines/rev.

<u>Example product code:</u>
5720/00/000/00/0000000/1000/1000

This is a 5720 configured as a factory default with 1000 pulse/rev encoders.

4 INSTALLATION AND WIRING INSTRUCTIONS

4.1 INSTALLATION

The 5720 controller is designed to mount directly onto a flat surface by means of two M6 bolts. Details on fixing centres are given in section 2.3.

It should be noted that the 5720 has a rating of IP00 and is not suitable for mounting where there is direct user access or where some environmental hazard exists.

4.2 BASIC WIRING INSTRUCTIONS

The 5720 is 24V d.c. powered and so no special precautions are required for the power wiring. All control wires should have a cross-section of 1.5 sq.mm. for robustness, (0.75 sq.mm. Minimum within the enclosure). A substantial ground or earth connection should be made to the terminal of the controller. In addition it is most important that encoders / motors are earthed, the various earths being joined at a star point along with 0V within the enclosure. This star point should be as close as possible to the incoming earth cable.

4.3 CONNECTION OF FIBRE OPTIC CABLES

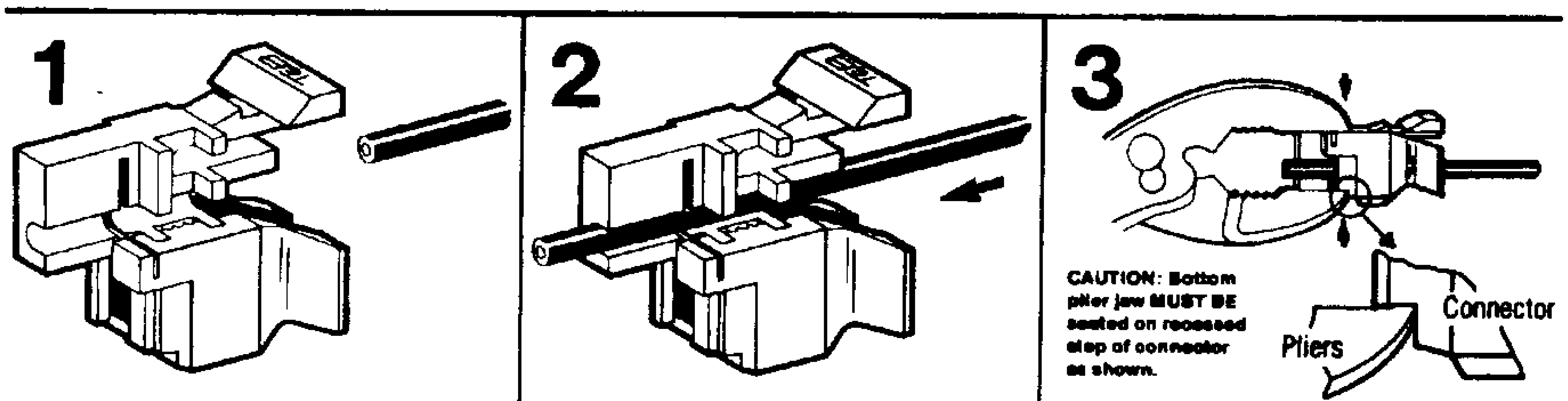
The 5701 MICROTACH and 5702 support products transmit their signal information via fibre optic cables. In addition to the fibre optic cables, two wires provide the auxiliary units with 24V d.c. power. The fibre optic cable and power wiring is daisy chained through repeater stages.

When using the fibre optic cable a number of things must be considered. Firstly use only 1mm plastic fibre optic cable specified by Eurotherm Drives. Other 1mm fibres may appear to be the same but may result in reduced system performance. When running the cable through trunking try to ensure that the black plastic coating is not damaged and that no heavy weight, such as large power cables, rests on the fibre. Lastly the minimum radius to which the cable may be bent is 1 inch or 25mm. If this bend radius is violated the fibre may not work. Alternatively, use the robust Eurotherm Drives composite cable, which contains a single fibre-optic cable and two copper wires, intended to convey 24v power to a Microtach.

Depending on the age of the 5720, the fibre-optic receiver will be one of two styles. Early versions use the Thomas & Betts plastic moulded style; later models use a proprietary steel type. Transmitters are all of the Thomas & Betts type.

The diagram below shows the simple three step procedure for terminating the fibre optic cable into a Thomas & Betts receiver. This termination process may be carried out in the field and requires no epoxy glue or polishing. The diagram is reproduced by permission of Thomas & Betts.

3-Step
Installation procedure The following is intended as a general description.



1. Connector plug is packaged ready to use. No fiber preparation necessary.
2. Insert the fiber in the connector as shown. The fiber should protrude through the housing a minimum of 1cm.
3. Press down the fiber clamp (using pliers) until it is fully bottomed in the housing. The termination is complete.

T&B

4.4 CONNECTION OF FIBRE OPTIC CABLES FOR ALL METAL RECEIVERS

The new receiver is effectively more sensitive, so in some applications the operating range changes to avoid overdriving the receiving. The table below shows the range for each transmitter.

TRANSMITTER	RANGE (metres)
5701	20 - 40
5702/1	20 - 40
5702/2	0 - 10
5702/3	20 - 40
5702/5	20 - 40
5702/6	20 - 40
5720	0 - 10
5703	0 - 40
LINK	Not affected

FIBRE OPTIC CABLE END PREPARATION

1. Fibre optic cable cutting kit (SSD part number LA385204) includes 1 off cutting fixture JA385201 and 1 off single edge cutting blade JA385205.

2. Insert fibre optic cable complete with sheath into cutting fixture and cut off with blade as illustrated in figure 1 and 2. For optimum results fibre optic cable should pass through both sides of block.

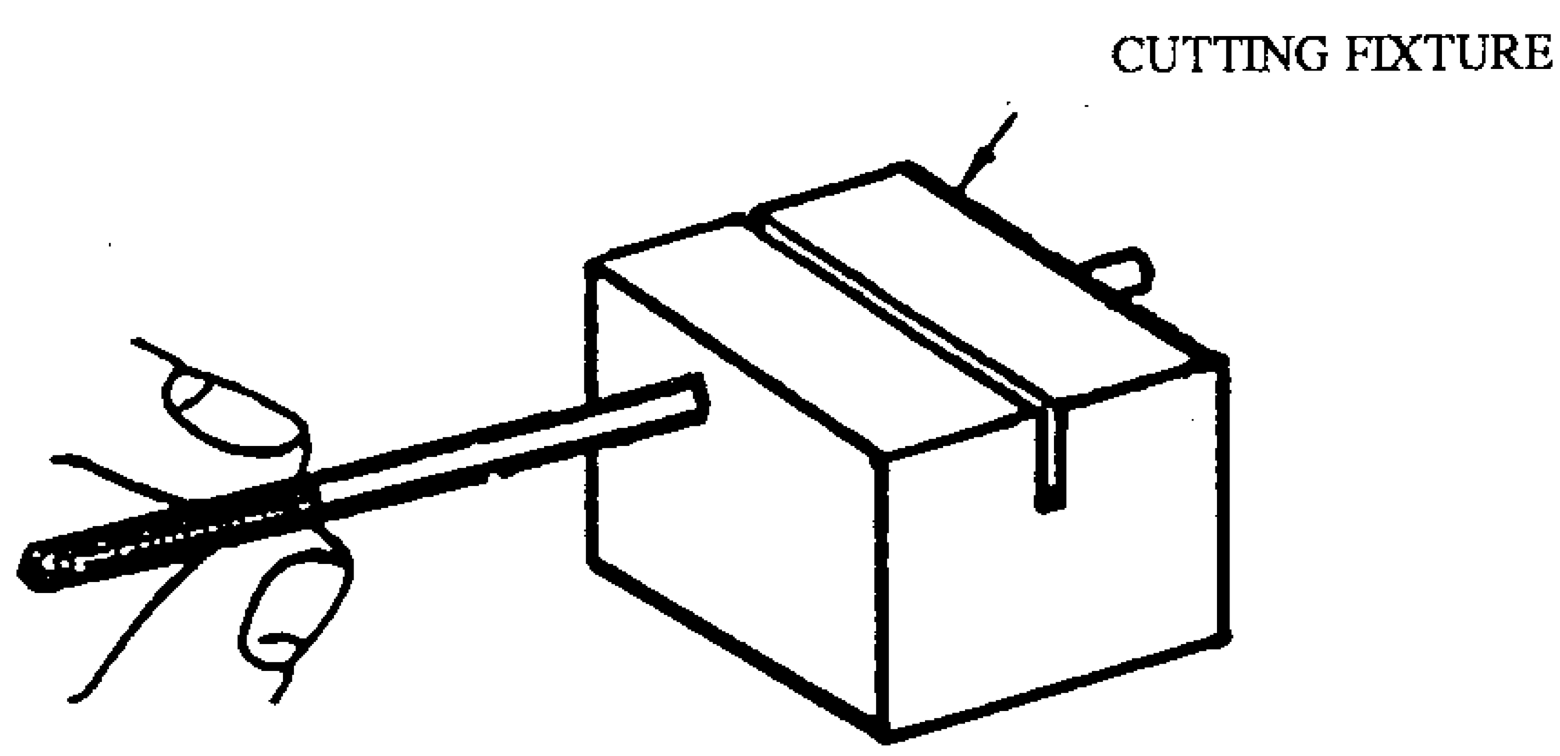


FIGURE 1

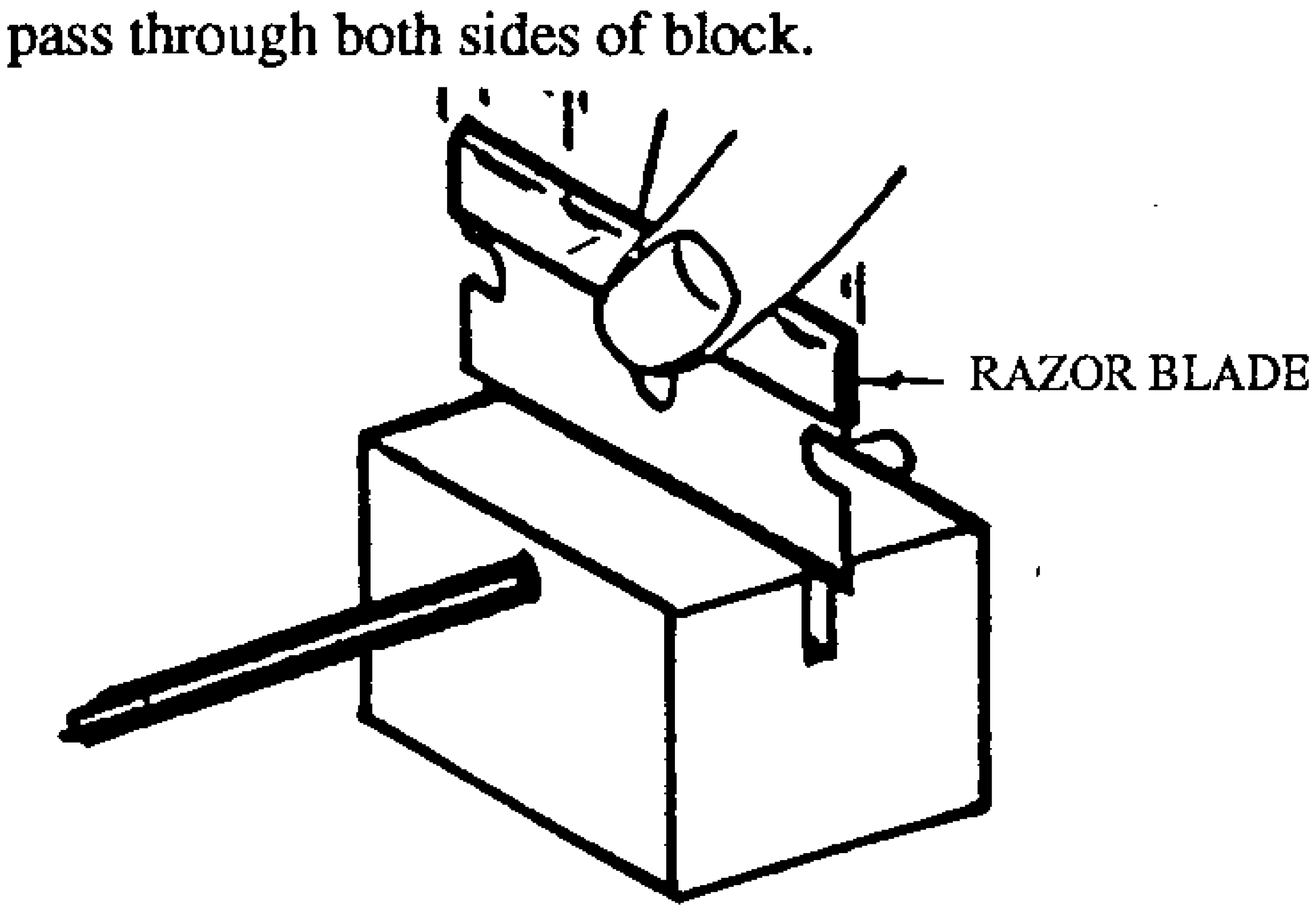


FIGURE 2

3. When using blade for second or more times try to select an unused section of cutting edge.

4. Care should be taken when discarding used single edge cutting blade.

5. When assembling fibre optic cable into connector sufficient axial pressure must be applied to maintain end of fibre optic cable in contact with electronic sensor.

6. Tighten both screws evenly to ensure metal to metal contact of connector housing.

5 THEORY OF OPERATION

5.1 SPEED AND RATIO CONTROL OF DRIVE SECTIONS

Speed control of a drive section is the basis for all control of production systems employing drives. Indeed the drive can only control speed and normally knows nothing of position or registration. The function of the 5720 is to maintain accurately slave shaft speed according to some reference source. To do this the 5720 measures the reference speed and compares it to the speed of the slave shaft, thus generating an error. The error is applied to a 'PI' function and the resulting output forms a speed trim to the slave drive.

The speed trim continuously adjusts the speed of the slave shaft to maintain the required relationship of reference and slave speeds. By using a trim of 10% maximum strength the loop is easy to set-up and unlikely to be unstable. In addition, the system may be run as a purely analog system by removing the speed trim from the slave drive.

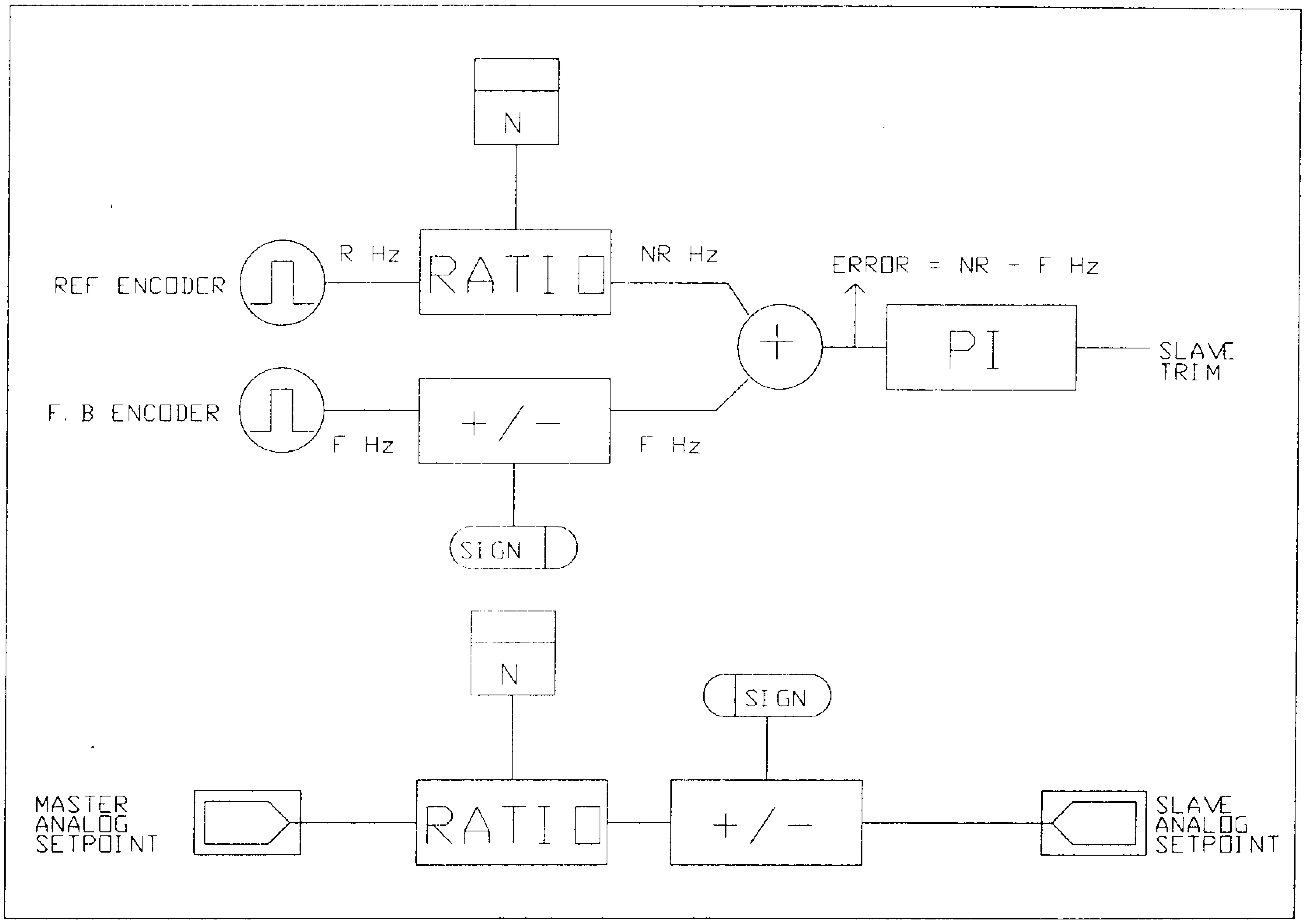


Figure 5. 1

As stated previously the function of the 5720 speedloop is to make the reference and slave shaft speeds equal. By adding some simple processing more elaborate results may be obtained. Consider figure 5.1. The reference encoder produces a frequency of R Hz and the slave encoder produces a frequency of F Hz. If the reference encoder frequency is multiplied by some factor N then the error will be:

Error = NR - F Hz.

As the 'PI' will null this error by applying a trim to the slave drive the slave drive will run at a RATIO of N times the speed of the reference drive. For example, if the reference encoder frequency is 21.45kHz and the RATIO is 1.25, the slave drive would run at a speed to produce an encoder frequency of 26.8125kHz. Although the speed holding accuracy of a drive may be only 0.1%, the speed-holding accuracy of the 5720 relative to a reference speed, and hence any drive using it, is absolute. The only limiting factor is the resolution to which the ratio may be set. On the 5720 the ratio may be set between the values of 0 and ± 1.999999.

The use of the sign changing block allows the slave motor to rotate in either the same or opposite direction to that of the reference motor. This is necessary as the loop takes account of the sign of the direction of rotation. If both motors normally rotate in the same direction the sign changer is not active, ie: the sign parameter is 0.

The reference drive speed is controlled by its analog setpoint. If we multiply this setpoint by the ratio value N the resulting value may be used as a setpoint for the slave drive. This allows the slave to run at approximately the correct speed, the trim then having only to make small corrections to that speed.

5.2 PHASE CONTROL OF DRIVE SECTIONS

Speed control, as detailed above, results in the steady state radioed speeds of the reference and slave shafts being equal. It should be noted that although the steady state speeds of the shafts are the same the two shafts will not have travelled through the same angle since rest. The speedloop PI will make the reference and slave encoder frequencies (or count values in our system) equal. To do this the reference shaft will move away from rest followed by the slave shaft. The difference in speed, caused by factors such as shaft inertia, will cause an error to be formed and the integral value to count up, this in turn causing a trim value to be applied to the slave shaft. While a speed difference exists between the shafts the integral value will increase. Once the two shafts are running at the same speed the integral value will stabilise. The resulting steady state trim will be due to mismatch of the analog set-points and mechanical variables such as friction.

In many applications the relative phase or angular displacement of the reference and slave shafts is important. These applications are termed phase control. The output trim from the speedloop is the phase error. ie: the value contained in the integrator is the difference between the angular positions of the two shafts since reset. If the speedloop trim is applied to a second PI and the output of that PI is used to trim the slave drive the phase PI will make the phase error zero and the two shafts will have moved through the same angle.

Thus converting a speed controller to a phase controller is simply a matter of adding an additional PI. Figure 5.2 shows the difference between the operating modes of speed and phase. In speed lock the slave shaft lags behind the reference shaft until the steady state speed is reached, when the two shafts will run at the same speed. In phase lock the slave shaft will again lag behind the reference shaft during acceleration but will move through an angle equal to the lag angle once steady state speed has been reached. The lag has been exagerated in the diagram to aid interpretation.

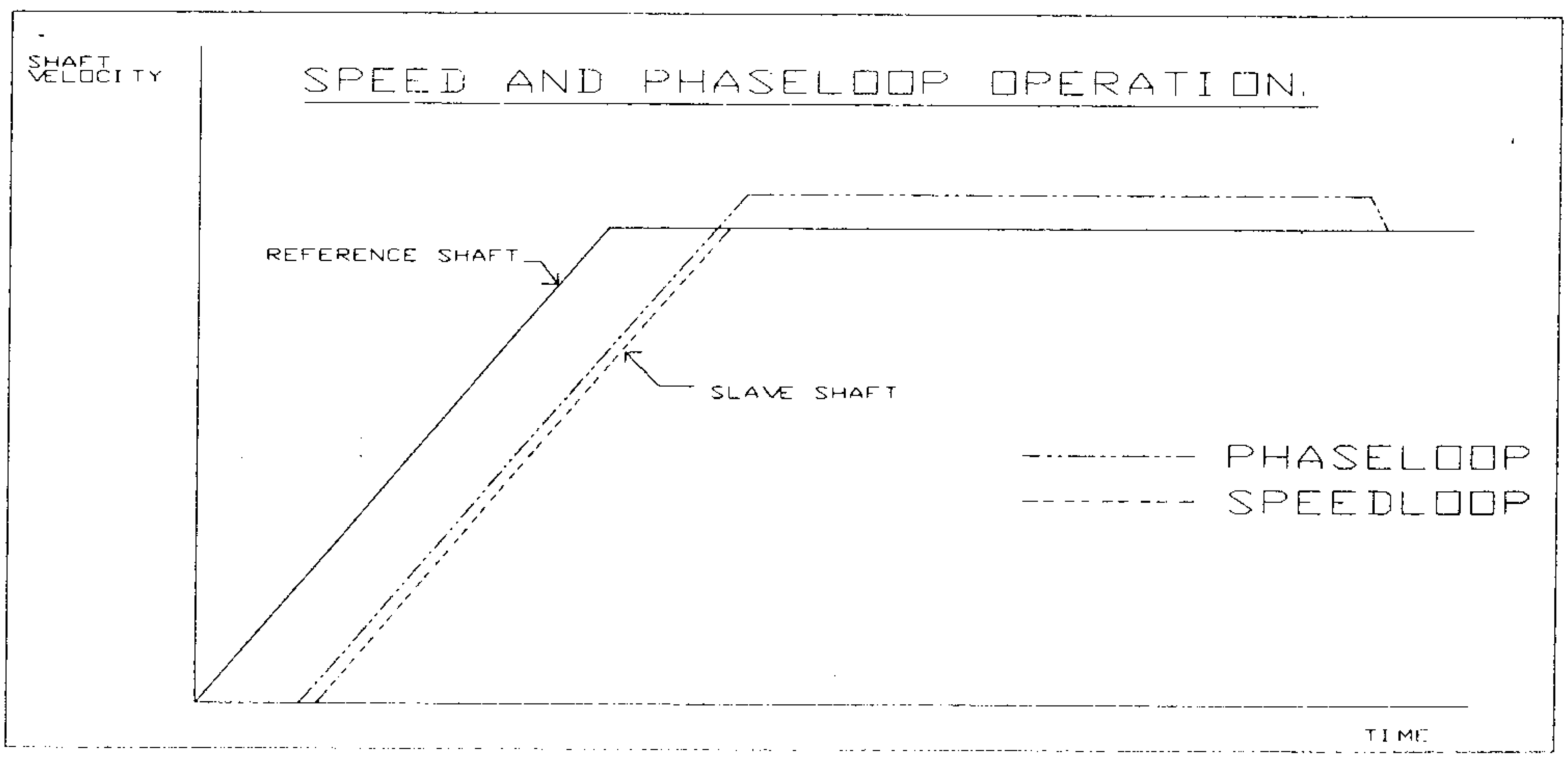


Fig 5.2

5.3 Register Control of Drive Sections

Register control is based upon the phase mode explained above. In the register mode the relative phase of the reference and slave shafts are controlled using the phaseloop. The phaseloop will lock the reference and slave shafts to a set but arbitrary position. By using the register loop the position of registration may be made absolute by using position marks.

The reference and slave marks may come either from the reference/slave encoders or from some external source such as an electric eye. The position of the reference and slave marks is compared and the error is entered into a PI function. This PI will force the error and hence the position displacement between the two marks to be zero. This is achieved by adding the register PI output to the position error of the speedloop. Thus the phaseloop will maintain the correct phase relationship between the reference and slave shafts with the register loop giving a once per repeat correction upon receipt of the marks.

To allow registration at some user defined point, independent of mark positions, the marks may be delayed electronically, allowing registration at any point of the revolution. If the phaseloop maintains accurately the phase relationship of the two shafts why is the register loop required at all? Whilst it is true that the phaseloop will lock the phase angle of the two shafts absolutely, it will do so only to the accuracy of the pre-scalers and ratios entered by the operator. Whilst these values may be set to an accuracy of six decimal digits, it may be impossible to set them accurately due to uncertainties in such things as roll diameters. If the ratio is not accurately set, the desired and actual phase position of the slave shaft will be different. By using registration marks the actual phase position is checked once per repeat and corrected if an error is apparent. Marks are also useful in applications where two shafts must always be registered in a certain position. By using marks the desired position will be achieved automatically without the need to rotate manually the shaft to the correct position on power up.

6 THE QUADRALOC BLOCK DIAGRAM

Figures 6.1 and 6.7 show the 5720 block diagrams. These diagrams consist of a number of blocks which together make a mode of operation. The main constituents of the block diagram are the speedloop, the phaseloop, the register loop, the analogue ratio blocks and the system functions. These blocks are combined in a fixed manner to form the required mode of operation.

6.1 THE SPEEDLOOP

This combination of blocks perform the basic speed locking process. The reference and slave encoder counts are pre-scaled to allow for different encoder resolutions, the reference encoder value is ratioed and the slave value may have its sign changed. The slave value is subtracted from the reference value to form the error. This error is then applied to a PI term and its output clamped. The clamped output is converted to an analogue value and used as a trim to the slave drive.

6.1.1 ENCODER COUNT SOURCES

The reference and slave encoders each provide a number or count value each time the software loop is executed. This count value is the number of counts that have been produced by the encoder during the loop time. The count value is dependent upon speed of rotation of the encoder and the resolution or number of pulses/rev of the encoder.

If the encoder has P pulses/rev (typically 1000 pulses/rev) and is rotating at N revolutions/minute, the count frequency is given by:

$$Count\ \ frequency\ = \frac{4\ P\ \ N}{60}\ counts\ /\ \mathrm{sec}$$

The number of counts per looptime is the count frequency multiplied by the looptime in seconds. It should be noted that the count value is signed, and therefore automatically takes into account the direction of rotation of the shaft.

The reference encoder value (D13) and the slave encoder value (D20) are only two of the three possible sources. The third count source (P24) is a parameter which may be selected as the reference count source instead of the reference encoder. To do this the switch parameter (P23) is set to be non zero. The fixed count source (P24) is used in place of the reference encoder when this is the first section of the machine and no reference encoder source exists. Operation of this mode is discussed in Section 6.3.

6.1.2 ENCODER PRE-SCALERS

The encoder count values may be pre-scaled by the reference and slave pre-scaler blocks. The scaling factors may be in the range 0 to 1.000000. The reference encoder value (D14) and slave encoder value (D21) are multiplied by the scaling factors (P25 and P33). The main function of this scaling is to accommodate for such things as different gear ratios and encoder resolutions on the reference and slave encoders.

The prime requirement is that the scaled values (D15 and D22) are equal at the maximum speed of operation. Although the scaling factor is limited to 1.000000, either the reference or slave encoder may be scaled and hence the higher frequency may always be made equal to the lower frequency.

6.1.3 RATIO BLOCK

The ratio block enables the speed difference between the reference and slave drive sections to be varied under user control. This is most commonly used to control draw between sections accurately. The ratio value (P27) may be between 0 and ± 1.999999 and is affected by the ramp function block.

6.1.4 RAMP FUNCTION BLOCK

The ramp function block is used to apply a controlled ramp to the ratio value. In many systems, especially those using gearboxes, a large instantaneous change in ratio may cause damage to the machine. By using a ramp function on the ratio this damage may be avoided.

There are up to nine inputs to the ramp function block: Ratio (P27), Ramp Gradient (P26), Halt ramp (D18) and Ramp quench (D17). On versions 2.12 and later there are also Digin Function (P82), Ramp Lower Limit (P83) and Ramp Upper LImit (P84). Ratio (P27) is the required ratio in the range 0 to ± 1.999999. The Ramp gradient value (P26) is the number added to the output of the ramp each loop time. This is not a ramp time but may be thought of as an acceleration limit. Using the operator station (5721) the ratio and ramp gradient values may be scaled for operator use. Thus ratio may be entered directly as a draw value and ramp gradient may be scaled so that a time in seconds may be entered directly on the operator station. Further details of these operations may be found in the operator station manual.

The halt ramp function causes the output of the ramp (D16) to be frozen at its current value independent of the set ratio value. The halt ramp function is active if D18 is non zero. D18 may be set by one of two sources, either digital input 1 (D43) or a serial link parameter (P30). Selection of D43 or P30 is controlled by the switch parameter P32. If P32 is zero the digital input is selected and if P32 is non zero the serial link parameter (P30) is used. D18 may also modify the sign of the ratio (see 6.1.3) on software versions 2.15 and later, so care must be taken in its use.

The ramp reset function is controlled by D17. If D17 is non zero the output of the ramp is reset to zero, if D17 is zero the ramp operates normally. Again the reset function may be driven by two sources, digital input 6 (D48) or the serial link parameter P29. Selection of the reset source is controlled by the switch parameter P31. If P31 is zero the digital input is used as the source and if P31 is non zero the serial link parameter (P29) is selected. The digital input (D48) works on the PI quenches as well. (These may be isolated using the switch parameters P42, P22 and P49).

If the digital inputs are used as the source for ramp reset and ramp halt, the input is in the same sense as the variable. Hence if ramp halt is required digital input 1 is high and the switch parameter P32 is zero.

On software versions 2.12 and later, there are five additional inputs. Digin Function (P82) controls the function of the inputs normally used for Inch Advance and Inch Retard (see section 6.1.9). In the default state (P82 = 0), Inch Advance and Inch Retard affect the inch block. If P82 is not zero, then these two inputs are disconnected from the inch block, and connected to inputs on the Ramp Function Block. In this state, Inch Advance (terminal B14) being true causes the ramped ratio (D16) to increment at the rate defined by Ramp Gradient (P26). Inch Retard (terminal B12) being true causes the ramped ratio to decrement at the same rate. There are clamps which limit the ramped ratio in this mode of operation. They are Ramp Lower Limit (P83) and Ramp Upper Limit (P84). Both clamps may take the range 0 ± 1.999999. The factory default values are Ramp Lower Limit = -1.999999, and Ramp Upper Limit = +1.999999.

On software version 2.15 and later, the sign of the ratio may be inverted by means of a digital or serial input. P85 selects if the inversion is controlled by digital or serial inputs. If P85 is zero, inversion is controlled by a serial input P86. If P85 is non-zero, inversion is controlled by digital input 1 (terminal B8). This digital input is also used to control the halt ramp function, so must be disabled by P32 if the invert ratio function is to be used.

6.1.5 FEEDBACK SIGN CHANGER BLOCK

The sign changer block allows the sign of the feedback to be changed. If the normal direction of rotation of the reference and slave shafts is the same the sign parameter P34 should be zero. If the normal direction of rotation is different then P34 should be non zero.

This operation ensures that the feedback speed value is subtracted from the reference speed value and not added to it. Operation may be confirmed by observing D12 and D19 which should have opposite signs.

6.1.6 SUMMING JUNCTION

The purpose of the summing junction is to add together the inputs to form an error. The summing junction has five inputs, the reference ratioed speed value D12, the feedback speed value D19, the trim inputs D27 and D28, and the speed offset P81. The result of the summing junction is the speedloop error D24. ie: D24 = D12 + D27 + D28 + D19 + P81.

The sign of the error (D24) may be changed using the parameter P36. If P36 is non zero the sign will be inverted. If the speed loop PI saturates, then change the error sign using parameter P36. In addition, if the error exceeds the number range the event will be flagged in variable D23. If an overflow has taken place D23 will be non zero, and an alarm will be flagged on the operator station (5721).

The speed offset input P81 serves the same function as an inch (see 6.1.9), i.e. to force the slave shaft to rotate at the reference shaft plus an absolute value, but it is a permanent offset, unaffected by any of the inch inputs. Also, it is a high resolution value, enabling very fine offsets to be made. The range of speed offsets is 0 ± 1000.000000. This is the value which is added to the speed error every loop time.

6.1.7 SPEEDLOOP PI

The speedloop PI is the control mechanism by which the 5720 maintains speed lock. The PI has six inputs and one output; two of the inputs are Boolean control parameters, two are gain factors, and two are saturation limits. The Boolean parameters control PI hold (P43), PI reset (D29), whilst the gain factors are for proportional gain (P37) and integral gain (P38). The positive and negative saturation limits are P70 and P71. Boolean diagnostic D2 is non zero if the integral value exceeds either of the saturation limits.

The control algorithm multiplies the error D24 by P38, the integral gain, and adds this result to the integral sum. The error D24 is also multiplied by the proportional gain P37 and this result is also added to the result. ie:

$$Output = Pgain \times Error + ((Igain \times Error) + Integral$$

$$= P37 \times D24 + ((P38 \times D24) + Integral)$$

D29 is the PI reset or PI quench function. If D29 is zero the PI works normally, whilst if D29 is non-zero the integral value and output are forced to zero. D29 may be driven by two sources, either a digital input or a serial link parameter. The choice of quench source is selected by the switch parameter P42. If P42 is zero, digital input 6 (D48) is used as the source, otherwise the serial link parameter P39 is used. It should be noted that digital input 6 (D48) is also connected to the ramp quench and other PI quenches. Care should be taken in isolating this parameter if the other quench functions are not required. Digital input 6 is high to quench.

P43 is the hold input to the PI. If P43 is zero the PI will function normally whilst if P43 is non-zero the PI will enter hold mode. In hold mode the output of the PI is set to zero while hold is active. During this active period the integral value is not updated but it is held. When the hold function is released the output is made equal to the held integral value and the PI is released to operate normally.

The number range of the integral value must not be exceeded or speed/phase lock will be lost. To aid the user in this respect, the number range of the entire speedloop is ± 1048576.999999. Two parameters provide positive and negative saturation limits. As the integral value is very large, the user may wish to know if the integral value exceeds a particular value. P70 is the positive saturation threshold and P71 is the negative saturation threshold. The value of P70 may be between 0 and 1048576.999999, and P71 may be between 0 and -1048576.999999. If the value of P70 or P71 is exceeded the speedloop PI saturation flag D2 will be made non-zero.

6.1.8 SPEEDLOOP CLAMP

The function of the speedloop clamp is to limit the absolute value of the trim. The positive and negative clamp values are independent and may be used to set asymmetric clamp limits. These are useful in machines which must not rotate in one direction. The positive clamp (P40) and the negative clamp (P41) have the number range 0 to 32767 and are both positive integers.

When the 5720 is configured as a speedloop the maximum trim value is limited to 8191 and hence P40 and P41 are limited to this value. (This is necessary to prevent overflow problems in the D to A converter). The clamped trim value is available on terminal C5, and may be added to the analogue setpoint if desired.

6.1.9 INCH BLOCK

The inch block applies a trim input to the summing junction (D28) when one of the two digital inputs is active or a direct position offset is loaded. The result of this trim is to cause an error which will cause the slave shaft to rotate by the appropriate amount. The gain of the inch block is variable and may be between 0 and 65,535. This is the value added to the error every looptime.

If ADVANCE is non zero (Digital input 4 is high) the value in P50 is output via D36 to the trim input of the summing junction (D28). If RETARD is non zero (Digital input 5 is high) the negated value of P50 is used as the trim. If both inputs are active simultaneously the trim is zero. A sign changer P51 is provided to change the sign of the trim value. This allows the user to inch the shaft in either direction using the ADVANCE and RETARD inputs.

The inch block may be controlled by the host serial link or the operator station using parameter P52. If P52 is zero the inch output is controlled by the digital inputs as described above. If P52 is non-zero, the digital inputs have no effect. Under these conditions the output of the inch block (D36) is equal to the inch gain (P50). The sign of the trim and hence the inch direction may be controlled by the inch sign (P51). The ADVANCE AND RETARD digital inputs may be disabled by making P52 non-zero and setting the inch gain (P50) to zero.

The output of the inch block is selected to drive D28 if the switch parameter P74 is zero. If P74 is non-zero the direct offset parameter (P75) is used to trim D28 in place of the inch block. P75, the direct offset parameter is a one shot offset load facility, i.e. if one revolution of the motor is 4000 counts and we wish to displace the shaft by 90 degrees, we should load an offset of 1000. Instead of gradually inching the shaft around we can select P75 and enter a value of 1000. This value is entered only once and is then cancelled. The range of P75 is 0 to 65,535 and the sign of offset is controlled using parameter P51. If P51 is zero the offset is positive and if P51 is non-zero the offset loaded is negative. The rate of direct offset may be controlled by parameter P6, direct offset gradient. If P6 is, for example, 24, and a direct offset of 1000 is entered, then the direct offset block will add a value of 24 into the speed loop summing junction on 41 successive loop times, and finally it will add a value of 16. Thus the total offset will be (41 x 24) + 16 = 1000.

In the register mode the inch block is inoperative. In this mode the advance / retard digital inputs control the delay of the register marks directly. This operation gives the same effect as inching in speed / phase lock but will not work at zero speed.

On versions 2.12 and later, the advance and retard inputs may be disconnected by means of parameter P82 (Digin Function). In the default state (P82 = 0) the advance and retared inputs are connected as described above. If P82 is not zero, then the advance and retard inputs are disconnected from the inch block, and are connected instead to the ramp block (see section 6.1.4).

6.2 THE ANALOGUE RATIO BLOCKS

The function of the analogue ratio blocks are to scale the reference drive setpoint with the same ratio as the reference encoder pulses. This scaled or ratioed setpoint is then applied as an analogue setpoint to the slave drive. The system of separate set-points and trims allows the slave drive to be run as an analogue system without the trim if required.

The 5720 has two analogue ratio blocks, one hardware and one software. The reason for two blocks is that we have two setpoint sources for the reference. The usual reference setpoint is the reference drive analogue setpoint. In this case the hardware analogue block is used to ratio the setpoint. The alternate source is the reference encoder, normally called tacho following. Here the reference encoder is scaled and used as the reference setpoint and the software analogue block is used to produce the slave ratioed setpoint.

6.2.1 THE HARDWARE ANALOGUE RATIO FUNCTION

If the reference analogue setpoint is used as the setpoint source this block is employed. The reference setpoint is connected to terminal C9. The analogue setpoint is ratioed using a multiplying D/A converter, the ratio being applied through either D16 or P80. D16 is the same ratio value as is used in the digital speedloop, whilst P80 is an independent ratio value. Selection of ratio source, D16 or P80, is achieved using the serial link parameter P79. If P79 is zero, D16 is used as the source whilst a non-zero value of P79 will select P80 as the source. The sign of the ratioed setpoint may be changed using P58.

The signed, ratioed slave setpoint may be added to the slave trim analogue voltage. To do this P59 must be non-zero. If P59 is zero the trim is not added to the setpoint. The hardware ratioed analogue output is present on terminal C3.

6.2.2 THE SOFTWARE ANALOGUE RATIO FUNCTION

If the reference encoder is used as the setpoint this block is employed. A filtered version of the reference encoder value (D14) is scaled using P53. The degree of filtering may be changed from 1 to 10000 using parameter P78. The time constant in seconds is given by the equation

$$Time\ \ constant\ = \ Filter\ \ constant\ \times\ 0.016$$

The scaling factor P53 is calculated so that the value of D14 at maximum speed results in a setpoint of ± 10000 (this results in a 10V analogue setpoint. In general D39 = 1000/1V) ie: If the encoder is 1000 lines/rev and the maximum rotational speed is 3000 RPM, then given a looptime of say 10mS, the encoder would produce 2000 counts/looptime. Given that we require a scaled setpoint of 10000 the scaling factor must be 5.000000. In general, given an encoder of P pulses/rev, a maximum rotational speed of N RPM, a looptime of T seconds the scaling factor may be calculated by using the following formula:

$$P53 = \frac{10000}{\frac{N}{60} \times 4 \times P \times T}$$

$$= \frac{150000}{N \times P \times T}$$

The scaled setpoint is used as the input to the software analogue ratio block. After a switch, the setpoint (D39) is ratioed using either the ramped ratio factor D16 or the independent ratio P60. The selection of ratio source is made using the serial link parameter P61 as described in the hardware analogue loop above. The sign of the ratioed setpoint may be changed using P56. If P56 is zero no inversion takes place, non-zero values of P56 invert the setpoint. The signed, ratioed setpoint is then clamped to prevent overflows and applied to a summing junction. The other input of the summing junction is D42. D42 is the output of a switch controlled by P57. If P57 is non-zero the trim value is added to the ratioed setpoint. If P57 is zero the setpoint is not added to the trim. The output of the summing junction (D37) is converted to an analogue voltage and is present on terminal C7.

P54 controls the selection of the source of the software analogue loop. If P54 is zero the scaled reference encoder value is used, as described above. If P54 is non-zero the parameter P55 is used. This would be required if the system were configured as a speed reference system. (See section 6.3).

6.3 QUADRALOC USED AS A SPEED REFERENCE SYSTEM

If the first drive in a system must run at a very accurate speed then a 5720 may be used to control that drive's speed using a speed reference or 'digital pot'. As the first drive has no master to follow, the master must be simulated. Two inputs must be provided for the 5720, the analogue setpoint and the reference encoder value, P55 and P24. These two software values may be programmed by the user directly or through the operator station as a scaled value such as percentage linespeed.

Selection of the normal reference sources or the simulated inputs are controlled by two parameters P23 and P54. If P23/54 is zero the normal reference sources are used, whilst a non-zero value of P23/54 selects the simulated values P24 and P55 as the reference source.

Selection of values for P24 and P55 is quite simple. Both parameters are set for the equivalent maximum line speed. The analogue setpoint parameter P55 is set to give a 10 volt output with a ratio of 1. The value of P55 required to produce 10 volts is 10000 and normally P55 is set to this value independent of speed. (Obviously, if the slave drive were scaled such that maximum speed was a voltage other than 10 volts P55 would need to be changed accordingly).

The value of P24 is speed dependant. The value used is the equivalent count value that would be seen from an encoder rotating at maximum line speed. Given a maximum line speed of N RPM, a resolution of P pulses/rev and a loop time of T seconds, the value of P24 would be:

$$P24 = \frac{N}{60} \times 4 \times P \times T$$

This speed reference system should only be used for a single drive system; if more than one section is required to run from the same setpoint the same external reference must be applied to all units.

It is important to realise that this method of speed referencing does not product an absolutely accurate speed reference. The summing junction calculates the difference between a parameter value and a speed measurement. The parameter value is absolutely accurate, but the accuracy of the speed measurement relies of the 5720's crystal oscillator. This has an accuracy of ±0.01%, so this method of speed referencing will produce a speed accurate to ±0.01% relative to the maximum speed.

6.4 EXAMPLE SPEEDLOCK SYSTEM

Consider a typical speedlock application shown in figure 6.4. This is a simple draw system employing two drive sections to provide a ± 9% draw to the web. To make the application more interesting certain limitations will be placed upon the design.

The reference motor is required to rotate at 3000 RPM at full speed. At this rotational speed the web will travel at X meters/min. The slave motor and gearbox is scaled such that at X meters/min the rotational speed of the slave drive is 2745 RPM. The slave drive is still a 3000 RPM motor with 10volts giving 3000 RPM. By scaling the motor to run at 2745 RPM at full line speed, the slave may apply a continuous draw of 9% without overspeeding.

The analogue ratio, assuming the drives are scaled for 10V = 3000 RPM, is 2745/3000 = 0.915000 = P27. This gives a scaled and ratioed frequency of 187 kHz for both reference and slave, thus the system will lock correctly.

The reference encoder has 1000 pulses/rev whilst the slave encoder has 1024 pulses/rev. Given a reference speed of 3000 RPM and a slave speed of 2745 RPM the equation in section 6.1.1 tells us the reference encoder frequency is 200 kHz and the slave frequency is 187.392 kHz. As the ratio is set to 0.915 for the correct analogue setpoint, the ratioed reference frequency would be 183kHz. As the reference and slave frequencies are different resolutions, the encoder pre-scaler may be used to null this effect. The slave frequency is higher than the reference, so the slave encoder must be scaled down. The scaling factor for the reference encoder is 183/187.392 = 0.976563 = P33. As a point of interest, this is exactly equal to the ratio of encoder resolutions, 1000/1024. In this example, the ratio cancels out in the equation, but as a general rule, it is best to be rigorous in the scaling factor calculations.

As the slave motor rotates in the opposite direction to the reference motor, the sign of the feedback frequency (P34) and analogue ratioed setpoint (P58) must be inverted. Both P34 and P58 are set to be non-zero.

An additional restriction could be that the system must not run in reverse due to the construction of the gearboxes. Assuming the reference setpoint is 0 to 10 volts, the trim setpoint will be 0 to -10 volts. To prevent the slave drive reversing the trim must not be positive, thus the positive speed clamp (P40) must be set to zero.

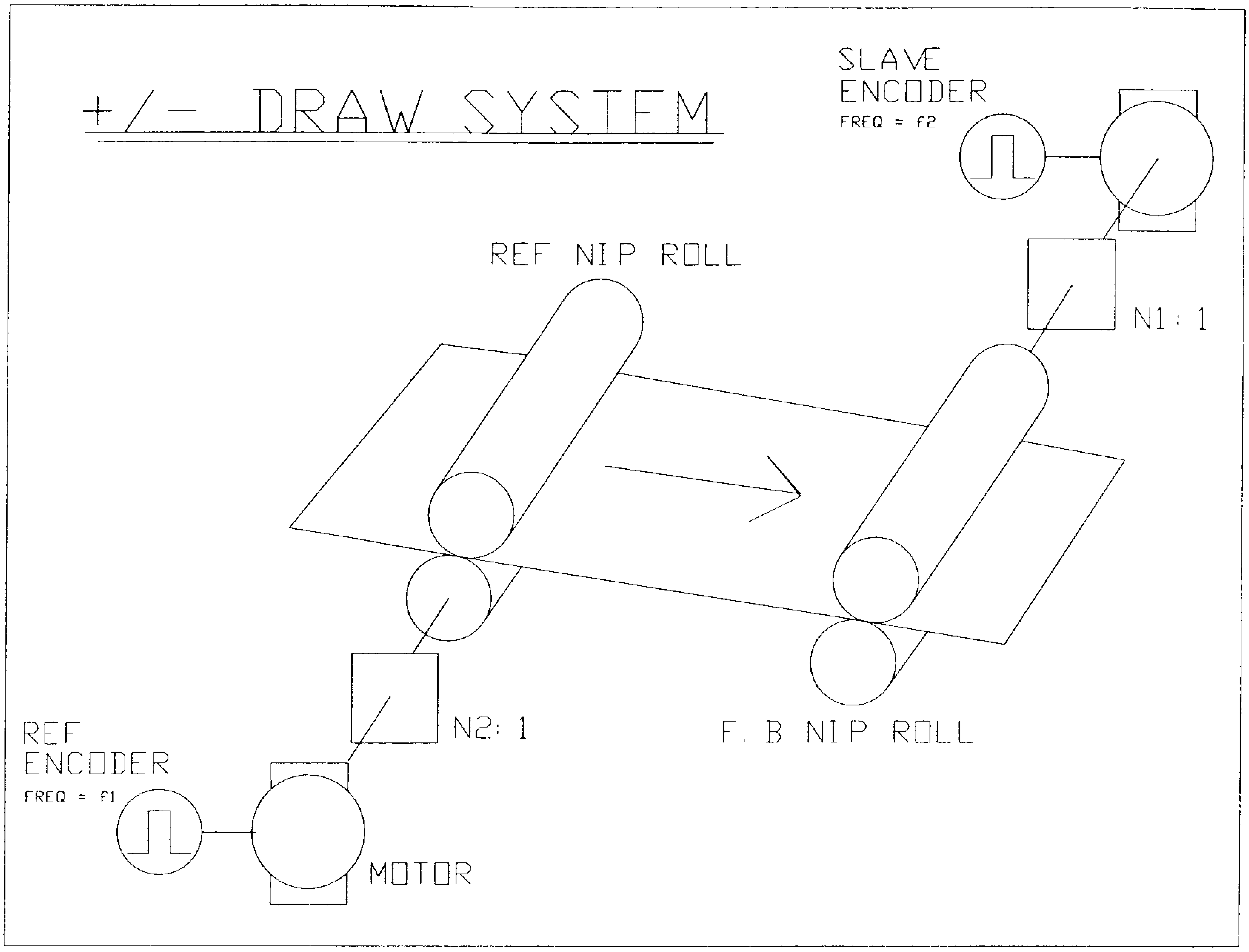

+/- DRAW SYSTEM
SLAVE
ENCODER
FREQ = f2
REF NIP ROLL
N1 : 1
N2: 1
F. B NIP ROLL
REF
ENCODER
FREQ = f1
MOTOR

Fig 6. 4

The set-up described above defines the operating point with no draw. ± 9% draw may be set by changing the ratio from 0.915000. Increasing the ratio will increase the speed of the slave drive and give positive draw; reducing the ratio will have the opposite effect. The operator station may be configured so that an operator may change the draw to say -3.5% and the operator station will set the correct value into the ratio (P27). This would be done by using the ranging and scaling facilities of the operator station. A 1% draw means changing the ratio by 0.01x0.915=0.00915. Thus if we wish to enter the draw in percent using the operator station (5721) the user name could be set to SECTION DRAW, the units would be % and the formula would be aX + b with 'a' set to 0.000915 and 'b' set to 0.915000. Thus if the operator sets a draw of -3.5% the ratio value (P27) would be set automatically to 0.911797.

6.5 THE PHASELOOP

The phaseloop is an addition to the basic speedloop of the 5720. All the parameters and features already mentioned are still present and function in the same way with the exception of the speedloop clamp. The phaseloop is a speedloop block diagram with an additional PI and clamp added after the speedloop clamp. (See figure 6.1). The speedloop clamp no longer drives the analogue output on terminal C5, but instead feeds into the phase PI. The output of the phase PI is clamped and then converted to an analogue voltage and is available on terminal C5. Maximum trim strength is still set to 8%. As with the speedloop, the trim signal may be added to the analogue slave setpoint.

The addition of the phase PI and clamp causes the position error produced by the speed PI to be nulled. Thus the phase or position error between the reference and slave shafts is reduced to zero. The use of the Inch advance/retard function allows position offsets to be entered directly.

6.5.1 THE PHASELOOP PI

The phaseloop PI is a simple 16 bit PI using the same algorithm as the speedloop PI. The speedloop position error D26 forms the input to the PI whilst the phase proportional gain is P44 and the phase integral gain is P45. Hence the operation of the phase PI may be described by the following:

Output = $(P44 \times D26) + (P45 \times D26)$ + Integral

The integral value is only 16 bits including sign, giving a range of ± 32767. The phase PI does not have the PI hold function but retains the PI quench. The PI quench is controlled by one of two possible sources, digital input 6 (D48) or the serial link parameter P46. Switch parameter P49 controls source selection. If P49 is zero the digital input is selected, otherwise the serial link parameter is used. As with the speedloop PI a high on digital input 6 or a non-zero value of P46 will cause the PI to quench. It should be noted that parameter D33 is inverted with respect to parameters P46 and D48. ie: Quench will take place if D33 is zero. This transformation is automatic and requires no user intervention.

Although the phase PI has no hold function, it does have a saturated integral flag. (D30). This flag will be zero during normal operation and will be non-zero if the integral overflows.

6.5.2 THE PHASELOOP CLAMP

The phaseloop clamp input is D31, the output of the phase PI. The clamp has two clamp limits, the +ve clamp limit P47 and the -ve clamp limit P48. The two clamps are independent and may be set between 0 and 8191. The output of the clamp (D32) is converted to an analogue voltage which is present on terminal C5. This trim may be added to the slave drive analogue setpoint as described in section 6.2.

6.6 THE REGISTER LOOP

The Register loop is an addition to the 5720 phaseloop block diagram shown in Figure 6.1 and is depicted in Figure 6.7. The function of the register loop is to allow phase synchronisation of the reference and slave shafts at an absolute position. The required absolute position is defined by register marks for the reference and slave channels. These register marks may be the zero index marks of the reference and slave encoders or they may be derived from some external source such as an electric eye.

A mark delay facility is provided so that the point of registration may be changed to any point in one revolution.

6.6.1 MARK INPUTS

Identical channels are provided for the reference and slave mark inputs. Both the reference and slave marks may be derived either from the relevant encoder or from an external mark source, giving four mark sources in all. Either the encoder or external mark may be used as the input to a delay unit, selection of the input to be used is controlled by the serial link parameters P1 (for the reference channel) and P7 (for the slave channel). If P1/P7 is zero the encoder is selected as the source, whilst if P1/P7 is non-zero the external mark is selected.

The delay unit is used to allow one of the marks to be delayed. If the clock used for the delay is from an encoder then the clock frequency will be proportional to speed and a constant value of delay count will result in a delay by a constant angle. Using this unit it is possible to delay one of the marks by up to one revolution and hence obtain registration at any point in the cycle. The accuracy with which registration can be set will depend upon the number of delay counts / mark.

The clock for the delay unit is derived from the 5701 Microtach.

The delay unit has four inputs. The selected mark (encoder or external) and the clock source are two. The other two inputs are the delay value and resolution. The delay value (P3 for the reference and P9 for the slave) is simply the number of counts we wish to delay by. The resolution (P4 for the reference and P10 for the slave) is the number of encoder counts / mark. Figure 6.7.1 shows how the delay unit works. The delay unit has a range of 20 bits allowing a maximum delay value of 1048575 counts. Assume we are using the standard microtach (5701) as the source of both the mark and the clock. The 5701 has 1000 pulses / rev, counting both A and B quadrature signals and counting rising and falling edges this gives 4000 counts / rev, thus the resolution value (P4,P10) would be set to 4000. Suppose we wish to delay the mark by 32 degrees. This corresponds to a delay of 356 counts, hence the delay value (P3,P9) would be set to 356. If we examine the left hand picture in figure 6.7.1 we can see that a delay of +356 counts is the same as a delay of -3644 counts. (Resolution = 4000 counts). Thus if we have two trigger limits, one of +356 and one of -3644 the direction of rotation of the shaft is irrelevant. If the shaft reverses we will still register to the correct point. This is the situation shown in the right hand diagram of Figure 6.7.1. Even though the maximum delay value is set at 1048575 we have set trigger limits of +356 and -3644. These two trigger limits are calculated automatically from the delay and resolution values entered above.

Once the resolution figure has been entered during commissioning only the delay figure need be changed. Using the ranging and scaling facilities of the 5721 operator station, this delay value may be entered by the operator in engineering units such as mm or degrees. The minimum value of delay may be zero.

On versions 2.12 and later, the reference resolution may be optionally controlled by the feedback resolution. The purpose of this is to enable only one parameter to be changed when the repeat length is changed. Otherwise two parameters would need to be changed, which is inconvenient for the operator when using a 5721. This feature is controlled by parameter Select Ref Res (P12). In the default state (P12 = 0) the actual reference resolution is simply the value of the parameter entered at P4. If P12 is not zero, then the actual reference resolution is equal to the feedback resolution (P10) multiplied by a scaling factor. The scaling factor is accessed as parameter P28, and the actual reference resolution (either P4 if P12 = 0 or P10 x P28) may be access as D58. The default value of scaling factor is 0.

When operating in register mode, the inch advance (Digital input 4) and inch retard (Digital input 5) directly affect the mark delay. Thus register may be obtained either by entering a delay directly using the delay parameter or by using the advance / retard digital inputs. It should be noted that the advance / retard digital inputs only affect the slave delay value (P9).

Either the non-delayed mark or the selected delayed mark may be used as the source for the register loop. This is done using the serial link parameters P5 (for the reference) and P11 (for the slave). If P5/P11 is zero the non-delayed encoder mark is used, else the delayed mark is used. (The non-delayed mark may be either a Microtach or external mark. This selection is made using Jumpers J1 and J3).

Either the reference or slave marks (or both) may have windows applied to them. The window feature is turned on/off using the parameters P65 and P66 (for the reference and slave channels). If P65/P66 is zero the window feature is disabled. Windows are a method of eliminating the effects of noise pickup on the mark channels. Extra mark pulses may be generated by dirt or spurious marks on a web and picked up by an electric eye. To prevent the register loop mis-triggering on these extra mark inputs the window feature will ignore any extra mark inputs occurring while the mark window is closed, which occurs after a valid mark. The window is then reopened for the rest of the cycle so that the next valid mark may be captured. This feature is implemented in hardware using the two custom gate arrays. The window size is controlled by parameter P68 for the reference mark and P69 for the slave. The value of the window may be 0 to 1.000000 revolutions programmable in steps of 0.000001. It is recommended that the window is never set to be greater than 0.95 as this may prevent capture of the next valid mark event.

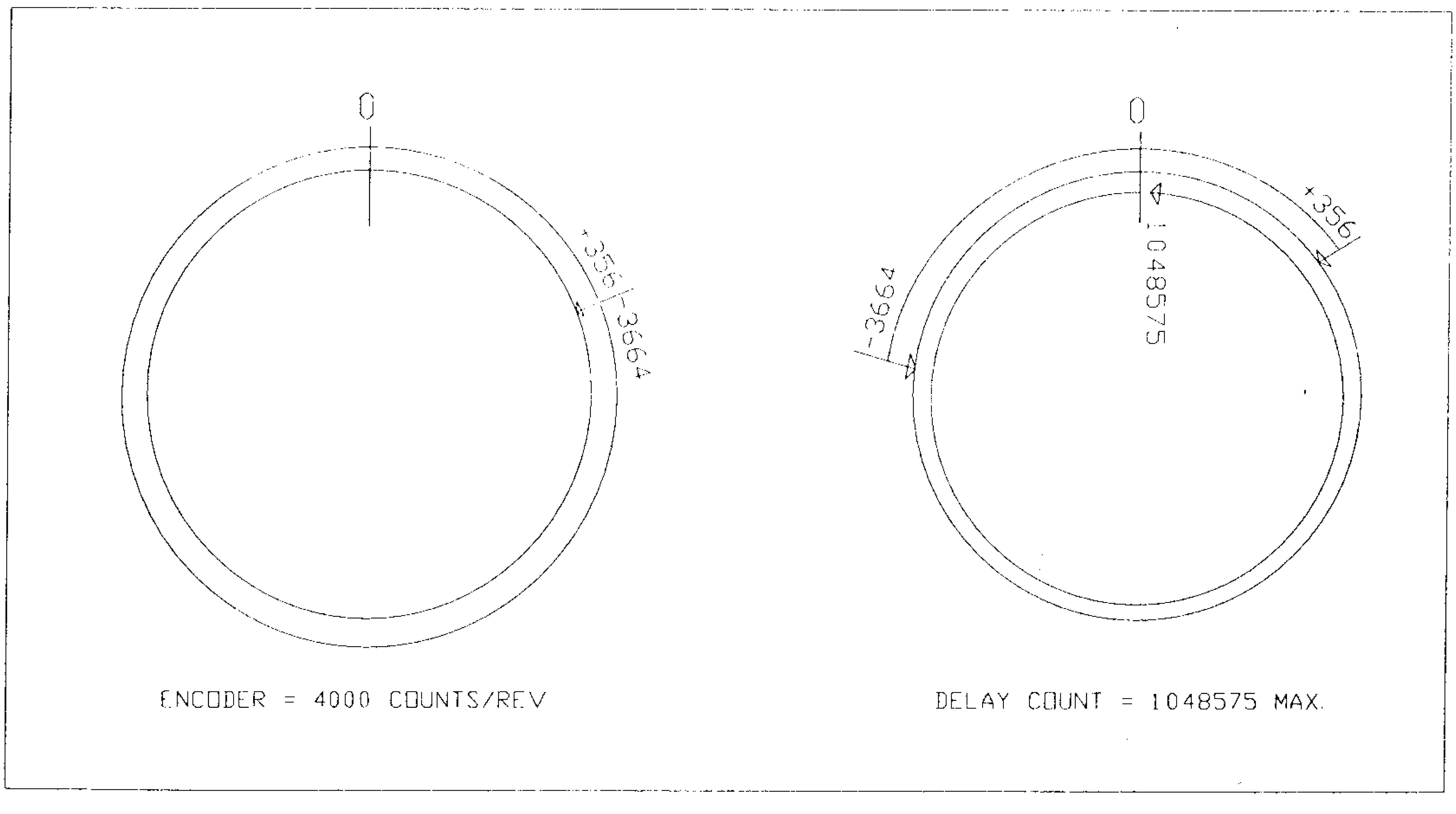


Fig 6.7.1

On each channel (reference and slave) the window feature uses the same delay hardware in the custom gate arrays as the marker pulse delay feature. It is therefore necessary to select delayed marker pulses (P5/P11 non zero) in order for the window to operate. Since the same hardware is used, it is not possible to both window and delay the marker pulse on one channel. However the reference and slave channels are independent, so that it is possible, for example, to apply a window to the reference channel, and a delay to the slave channel. If the window feature is enabled, any attempt to modify the delay value for that channel is ignored.

It should be noted that a high mark signal holds the delay circuit in reset. The delay does not start until the mark falls. The maximum delay/revolution is thus reduced by the width of the mark pulse.

6.6.2 ERROR GENERATION AND NORMALISATION

Once the reference and slave marks have been delayed or windowed, the slave 'time of arrival' is subtracted from the reference 'time of arrival', the result of this operation being the error. At this point the error is a time. This time is normalised to be a percentage of one revolution using the normalisation block. This operation is done automatically, the result being the error which is fed into the register loop.

Normalisation is performed by using the ratio of the current speed and the maximum line speed. Maximum line speed must be entered as a variable and is programmed as the maximum count value in one looptime. (P13).

$$P13 = \frac{Max \quad speed}{60} \times 4 \times Encoder \quad resolution \times Looptime$$

where : Max speed is measured in RPM
Looptime is measured in seconds

6.6.3 MISSING MARK AND ZERO SPEED CONTROL

The function of the missing mark circuit is to compensate for deficiencies in the mark detection method. It is possible that a mark sensor may not see a valid mark event. This can happen when the sensitivity of an electronic eye has not been set correctly or if the image contrast is very low. Under these circumstances the eye sensitivity may have to be set to a level where it may occasionally miss a mark to prevent the unit mis-triggering and producing extra marks during normal running. Another possible cause is when a CI printing press is stopped the print cylinders will lift off at zero speed and may as a result fail to print one mark. An electric eye downstream would then see a hole where a valid mark should have occurred.

The missing mark unit effectively compensates for the missing mark by limiting the error produced. If no missing mark unit were present, a missing mark would generate an error of one cycle. The missing mark unit has a programable limit to the error. When the first mark event arrives, an error window is opened. (See figure 6.7.3). When the second mark event arrives the error window is closed and the error is formed. If the second mark event is missing the error is limited to the value of the missing mark window. Normally, this window can be set to a very small value. If we consider a coating application the specification may be to provide registration to ± 1mm with a 1m repeat length. If the error window exceeds 1mm then the registration system is out of synchronisation. If we set the missing mark window to say 2mm then the error will be limited to that value. We could of course set the window to 1mm but this would be dangerous. We know from the specification that the register may be upto 1mm out and if the second mark was not in fact missing but merely late, perhaps due to some unusual mechanical disturbance, then the register system would be unable to re-lock onto the mark as it would be outside the window set by the missing mark circuit. Thus the system would not be registering correctly and the missing mark circuit would be hiding the problem that actually exists.

We can see that the missing mark circuit is intended to protect against occasional errors. Obviously, if one of the marks is permanently missing no scheme will provide correct registration as there is no datum. To aid the user in setting the limits of the missing mark window an out of synchronisation flag is provided (D1). D1 is low for normal operation.

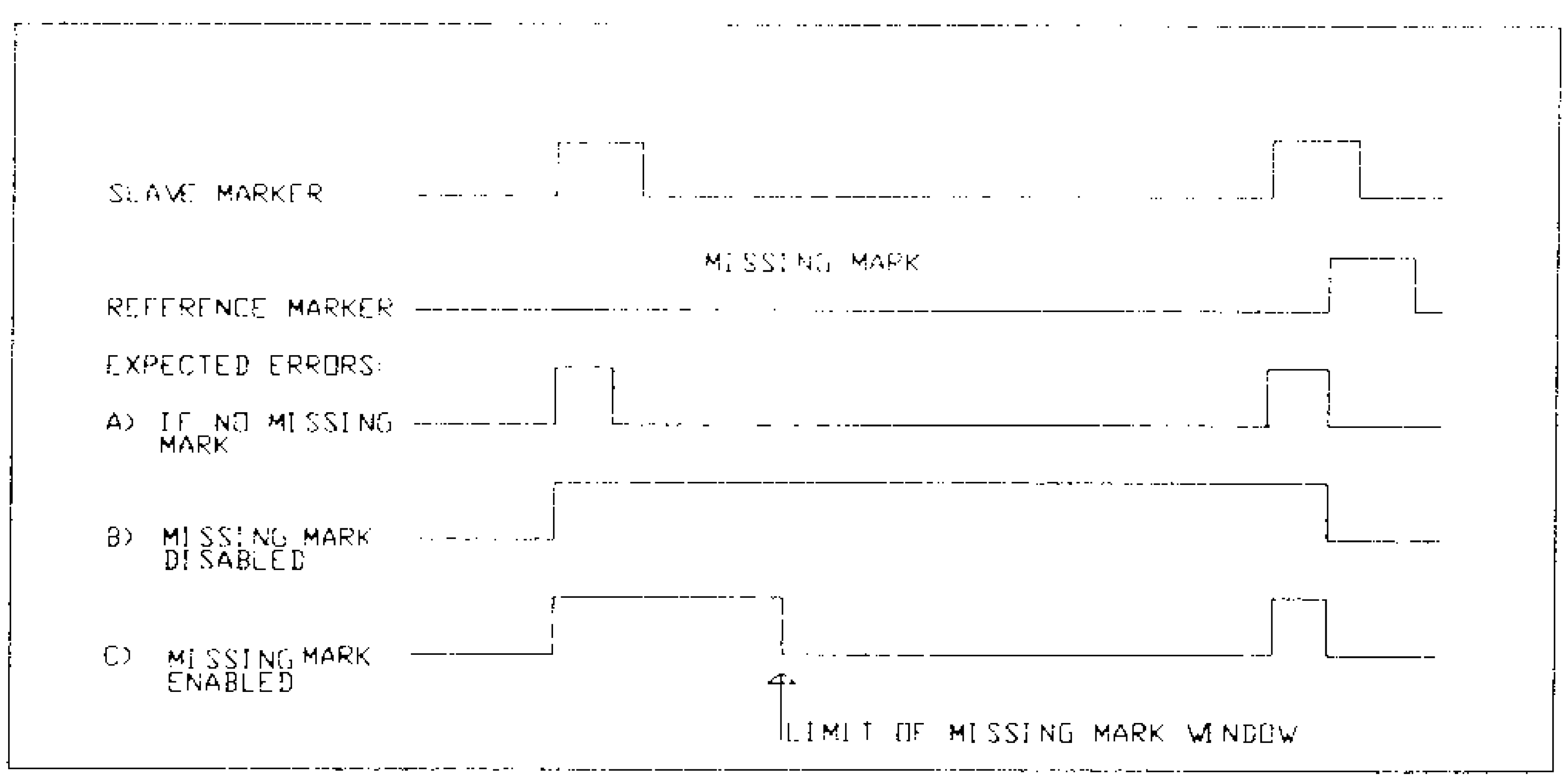


Fig 6.7.3

The missing mark facility may be disabled using parameter P15. If P15 is low the missing mark circuit is disabled, although the "out of sync" output is still true. Once the error returns within the missing mark window it must remain there for 8 cycles before "out of sync" goes false. If the error is greater than the missing mark window for more than 16 cycles "out of sync" remains true but the window limit is removed and replaced by actual error. This allows the system to regain lock. The disable flag (D6) is actually the result of combining P15 with D5. Only if both of these flags are true (non zero) will the missing mark unit be enabled. D5 is the zero speed flag. The average value of the reference speed (D4) is compared to a trigger threshold P62. If D4 <= P62 we say that the system is at zero speed. Obviously P62 may be set to values greater than zero (maximum value = 4095) so that a speed threshold value may be set. The actual value placed into P62 is the number of counts / looptime at the required threshold speed. Let us say that we wish the threshold speed to be 5RPM and we are using 1000 pulse / rev quadrature encoders giving 4000 counts / rev. Let the looptime be 10mS. The number of counts / looptime at 5RPM is:

$$\frac{5}{60} \times \frac{4000}{100} = 3$$

More generally, the value of P62 is given by:

$$\frac{\text{Speed threshold} \times \text{Counts / rev} \times \text{Looptime}}{60}$$

where : Speed threshold is in RPM
Looptime is in seconds

As we have combined P15 and the zero speed flag (D5), the missing mark facility will not work at 'zero' speed. This is intentional as when the drive actually stops, the time between two marks is infinity and under these circumstances a meaningful error cannot be produced. Because of this the missing mark unit and the PI are disabled at very low speeds. The minimum value of P62 is 1. Hence, using the above formula we can see that the minimum registration speed is 1.5 RPM using 1000 pulse/rev encoders and a 10mS looptime.

The missing mark window (P14) is the proportion of one repeat that the window is to remain open. The range of P14 is 0 to 1.000000. Thus given a 2m repeat length the possible missing mark window range would be 0 to 2m with a resolution of 0.002mm.

The zero speed signal is not only available using D5 but also appears as a digital output. (Digital output 2). This output is low if zero speed is true.

6.6.4 REGISTER LOOP SIGN CHANGER

The sign changer unit takes the error from the missing mark unit (D7) and produces the signed error D9. The parameter P19 controls the operation of the sign changer, if P19 is zero no inversion takes place.

6.6.5 REGISTER LOOP PI

The function of the register loop PI is to make the mark error (D9) zero. The PI uses the same algorithm as the speedloop PI and has the same number range. The PI proportional gain is P16 and the integral gain is P17. The output of the PI may be monitored using D8.

The PI is 'held' at zero speed to prevent large trims being generated when the drives are disabled. Zero speed hold is performed automatically; the threshold being set by P62 as described above. In addition the PI may be held at any other time by making P64 non-zero. When the PI is held the output of the PI is zero and any new error value is ignored. The integral value is however held, and when the PI is released from the hold mode this value is output.

In addition to the PI hold function there is also a PI quench. This function resets the PI integral and sets the output to zero. The PI may be quenched by two methods. Parameter P18 may be non-zero or digital input 6 may be high. The serial link switch parameter P22 controls the source of the quench. If P22 is zero the digital input is used, otherwise P18 is used as the source. It should be noted that digital input 6 is also used for other PI quenches as well as the ramp quench, thus care be used when selecting this input as the quench source.

The register loop PI also has a saturated output. If D54 is non-zero the PI is said to have saturated. The point at which 'saturation' occurs is programmable by the user. Parameter P72 sets the positive saturation limit whilst P73 sets the negative limit. The saturation level may be between 0 and 1048576 and the positive and negative limits may be asymmetric.

P76 is the PI auto de-gain factor. The auto de-gain feature is enabled by making P77 non-zero. If P77 is non-zero and the error is within the mising mark window (P14), we are in-sync and the register loop P and I gains are divided by the de-gain factor (P76). If out of sync is true (D1 is non-zero) the full strength PI gains are used. This system allows the use of high gains to capture the lock position and then low gains to reduce in-lock ripple.

6.6.6 REGISTER LOOP CLAMP

The function of the clamp is to limit the trim that may be applied by the register loop and to prevent overflow of the speedloop summing junction. Maximum trim may be ± 10000. The maximum value of trim may be reduced from this level by using the trim clamps P20 and P21. The value of the clamps are programmed as 16 bit 2's complement numbers. The clamp output appears on D10.

The output of the clamp forms one input to a switch, the other being the value zero. The function of the switch is to allow the register loop to be isolated. This is very useful during commissioning as the operation of the register loop may be observed without the trim causing movement of the slave shaft. Control of this facility is via parameter P63. If P63 is zero the register loop trim is connected, else the trim is zero.

6.7 SYSTEM FUNCTIONS

6.7.1 LOOP TYPE SELECTION

As described above, the 5720 is configured as a number of modes, each mode being a particular arrangement of blocks. Selection of the mode of operation or loop type is controlled by the loop type selection block. This block generates a variable (L1) which is used by the operating system to determine the required mode of operation or loop type.

Selection of loop type may be controlled by one of two sources, decoded digital inputs or a serial link parameter (L4). Control of the loop type source is via parameter L2. If L2 is zero the decoded digital inputs are used, otherwise the serial link parameter is used. The decoded digital inputs (L3) are driven by two digital inputs, D44 and D45. If neither digital inputs are high the mode defaults to speedloop. If digital input 2 (D44) is high the mode changes to phase. If digital input 3 is high (D45) the mode changes to register.

The digital inputs and serial link parameter (L4) are scanned every looptime and change of mode is possible during operation. It should be noted that due to the different block structures involved in different modes that bump-less transfer between modes may not be possible under all operating conditions.

6.7.2 DIGITAL OUTPUT 1 SELECTOR

Digital output 1 may be used to indicate the operational status of the 5720. This digital output may be driven from one of four sources, D2 the speedloop PI saturation flag, D1 the out of synchronisation flag, D30 the phaseloop PI saturation flag and D54 the register loop PI saturation flag. Digital output 1 is the inverse of the flags, i.e. it is low to indicate an error.

Selection of the source to drive digital output 1 is controlled using parameter P67. P67 has the values 0 to 3. If P67 is 0 then the phaseloop PI sat flag (D30) is sent to the digital output. If P67 is 1 then the out of sync flag (D1) is used. If P67 is equal to 2 then the register loop PI sat flag (D54) is used and lastly if P67 is equal to 3 the speedloop PI sat flag (D2) is used as the source of digital output 1. D2 is the default source.

6.7.3 OPERATOR STATION / HOST SERIAL LINK SELECTION OF VARIABLES

Either the operator station (5721) or host serial link may be used to observe diagnostics and change parameters. Indeed, both the operator station and the host serial link are RS422 EI ASCII Bisynch compatible serial links and both use the same mnemonics.

The operator station should be connected to terminals B1 to B17 as detailed in the operator station manual. Once the operator station has been connected the display will show the operator menu structure. Details on this structure and how to configure it are given in section 8.5. To exit this level of the menu and enter the engineering level press the E key. The operator station will now prompt you to enter a four digit password. The default password is 0. However, the password is user definable and may be changed. If you do change the password remember to keep a copy in a safe place as there is no other way of entering the engineering level of the menu, without service assistance.

The engineering level of the menu allows access to all the diagnostics and parameters available in the 5720. The exact structure of this menu is shown in appendix A. In addition to the diagnostics and parameter list there are entries for Alarms, Op-stn setup (MMI), Serial link setup, Parameter saving and Operator menu configuration. To move around the menu structure use the M key to go down a level (shown as left to right in appendix A), the E key go back up a level, whilst the up and down arrow keys move around within a level. When entering parameters the up and down keys toggle switch type parameters on and off. For numeric type parameters the value may be changed either by using the up and down arrow keys or by entering the value directly using the numeric entry keys combined with the enter key. Further details on the operator station and its operation may be found in the 5271 operator station manual HA058017.

When using a new operator station the configuration menu should be entered and the system device selected to be a 5720 Quadraloc, press "Enter" to confirm this choice. If the 5720 is also a new unit the parameter save menu should be entered and factory defaults selected. This will initialise the Quadraloc parameters and allow entry of changes using the "Setup Parameters" menu position.

The operator station displays the diagnostic and parameter names in English and no knowledge of the serial link mnemonics or variable limits are required. (The operator station automatically limits the value of parameters). The Host RS422 link does require the user to apply limits. The link requires an EI Bisynch compatible driver which supports the 5720 mnemonics. If the user wishes to address a particular diagnostic / parameter then he must know the mnemonic for that item. To find the mnemonic first of all identify the point of interest in the block diagrams (Figures 6.1 and 6.7). The item will possess a D number if it is a diagnostic (read only) or a P number if it is a parameter (read / write item). Having identified its P/D number find this in appendix B. Listed next to the number will be the mnemonic and the legal number range for that item.

6.7.4 LIST OF PARAMETERS AND LIMITS

Parameters and variables consist of two basic types, Boolean and numeric. Boolean types are logical flags and controls, they have two states, on/off, true/false. These states are described by the values non-zero and zero. Boolean types are shown on the block diagram as an oval parameter or variable. Numeric types have more than two values or states. Each numeric parameter or variable has a range of values given in the table. Numeric types are shown on the block diagram as a square or rectangle.

Boolean and numeric parameters are identified by a black bar through the symbol and a P number. Parameters are the inputs to the various blocks. Parameters include such things as ramp hold control inputs and inch gain. Variables, wether Boolean or numeric are the results of operations within the block diagram and are designated by a D number. Parameters may be read or written to by the operator station or serial link, whilst variables may only be read. This is shown on the block diagram by the R/W and R/O symbols attached to the parameters and variables.

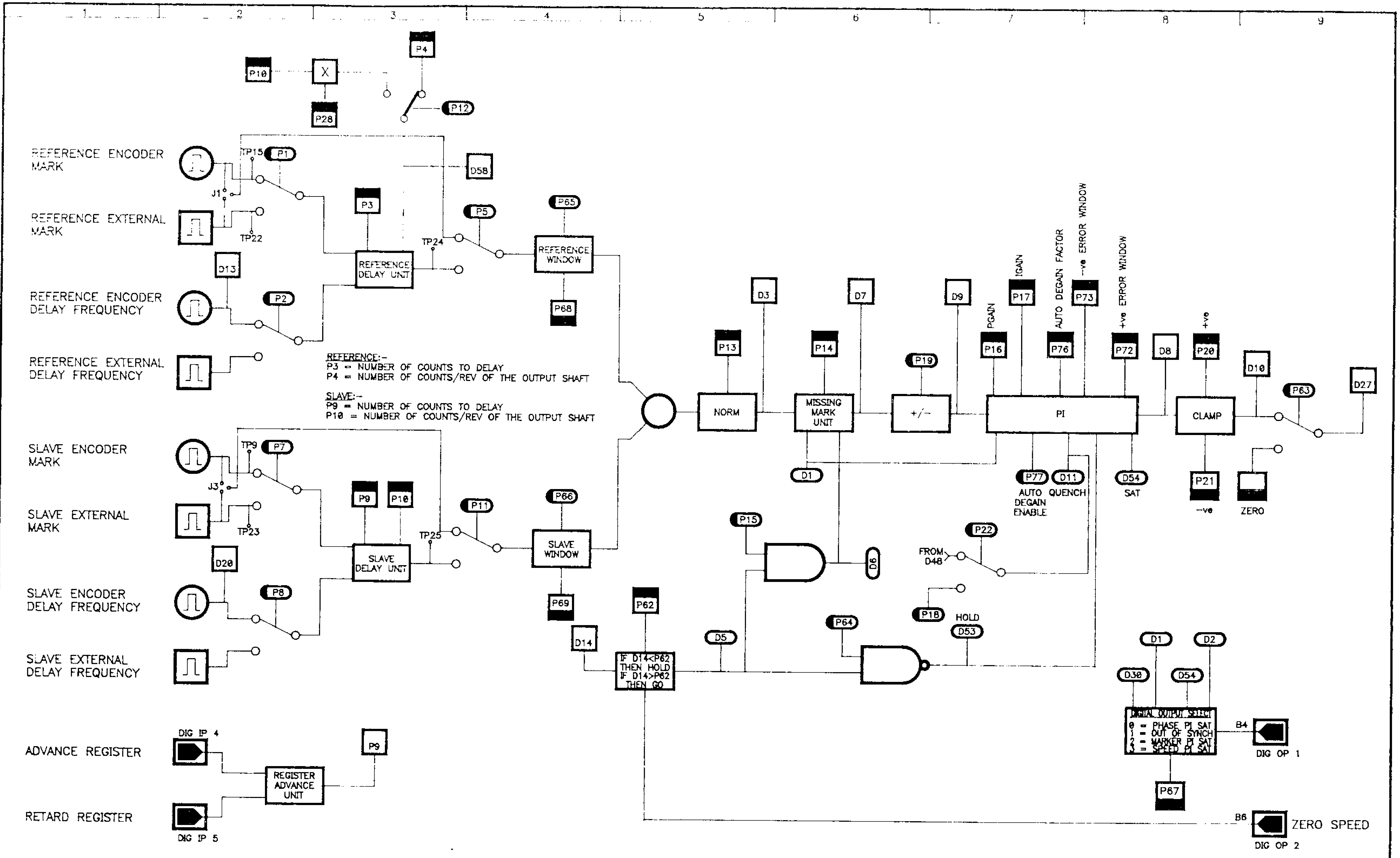


Figure 6.7

DRAWN	CHECKED	DATE						
DEB	AFL	20/3/90	10/4/90	10/10/90	3/12/90	13/02/91	15/10/92	30/11/92
TRACED	DESIGN APP.	ISS	A	B	C	1	2	3	4
MLE	DEB							

ELECTRICAL SYMBOLS GENERALLY TO BS 3939

EUROTHERM DRIVES Ltd.

TITLE: BLOCK DIAGRAM FOR REGISTER LOOP (Version 2.3)

USED ON: 5720

DRAWING NUMBER: HH 058184 D

SHT. 1 OF 1

KE085116 ISS. A

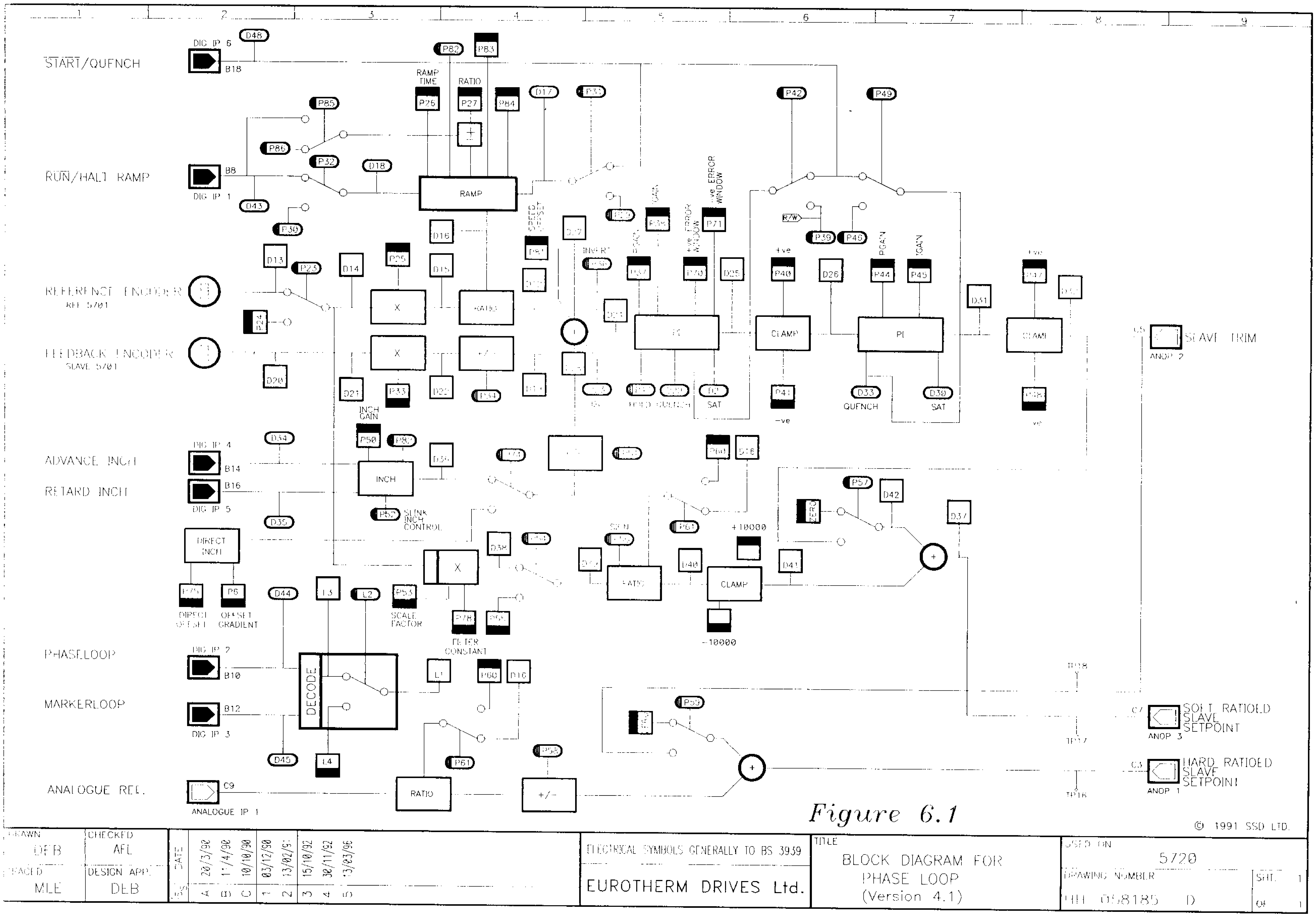

START/QUENCH
RUN/HALT RAMP
REFERENCE ENCODER
REF 5701
FEEDBACK ENCODER
SLAVE 5701
ADVANCE INCH
RETARD INCH
PHASELOOP
MARKERLOOP
ANALOGUE REF.
DIG IP 6
B18
DIG IP 1
B8
DIG IP 4
B14
DIG IP 5
B16
DIG IP 2
B10
DIG IP 3
B12
ANALOGUE IP 1
C9
RAMP TIME
RATIO
RAMP
INVERT
INCH GAIN
INCH
SLINK INCH CONTROL
DIRECT INCH
DIRECT OFFSET
OFFSET GRADIENT
SCALE FACTOR
FILTER CONSTANT
DECODE
RATIO
CLAMP
PI
+ve
-ve
PGAIN
IGAIN
SAT
QUENCH
+ve ERROR WINDOW
-ve ERROR WINDOW
+10000
-10000
SLAVE TRIM
ANOP 2
SOFT RATIOED SLAVE SETPOINT
ANOP 3
HARD RATIOED SLAVE SETPOINT
ANOP 1
© 1991 SSD LTD.
DRAWN DFB
CHECKED AFL
TRACED MLE
DESIGN APP. DEB
DATE
20/3/90
1/4/90
10/10/90
03/12/90
13/02/91
15/10/92
30/11/92
13/03/96
ELECTRICAL SYMBOLS GENERALLY TO BS 3939
EUROTHERM DRIVES Ltd.
TITLE
BLOCK DIAGRAM FOR PHASE LOOP (Version 4.1)
USED ON 5720
DRAWING NUMBER HH 058185 D
SHT. 1 OF 1

Figure 6.1

D No.	Range or value	Function
D1	zero or non-zero	Missing mark out of synchronisation 0 = in synchronisation Non-zero = out of synchronisation
D2	zero or non-zero	Speedloop PI saturation 0 = no saturation Non-zero = saturation
D3	±1048575.999999	Register loop normalised error
D4	±40000	Summed reference speed
D5	zero or non-zero	Zero speed 0 = zero speed Non-zero = not zero speed
D6	Zero or non-zero	Missing mark correction enable 0 = no correction Non-zero = correction enabled
D7	1048575.999999	Missing mark error output
D8	±1048575.999999	Register loop PI output
D9	±1048575.999999	Missing mark signed error output
D10	±10000	Clamped register loop trim
D11	zero or non-zero	Register loop PI quench 0 = no quench Non-zero = quench
D12	±19999.999999	Ratioed reference speed
D13	±10000	Reference encoder count value
D14	±10000	Reference speed input
D15	±10000.000000	Scaled reference speed
D16	0 to 1.999999	Ramped ratio value
D17	zero or non-zero	Ramp quench 0 = no quench Non-zero = quench
D18	zero or non-zero	Ramp hold 0 = no hold Non-zero = hold
D19	±19999.999999	Signed slave speed
D20	±19999	Slave encoder count value
D21	±19999	Slave speed input
D22	±19999.999999	Scaled slave speed
D23	zero or non-zero	Summing junction overflow flag Zero = no overflow Non-zero = overflow
D24	±39999.999999	Speedloop error
D25	±1048576.999999	Speedloop PI output
D26	±32767	Speedloop clamp output (Range = ±8191 if speedloop)
D27	±10000.000000	Speedloop trim input 1

D No.	Range or value	Function
D28	±10000.000000	Speedloop trim input 2
D29	zero or non-zero	Speedloop PI quench control Zero = no quench Non-zero = quench
D30	zero or non-zero	Phase PI saturated flag Zero = no saturation Non-zero = saturation
D31	±32767	Phase PI output
D32	±8192	Phase trim output
D33	zero or non-zero	Phaseloop PI quench control Zero = quench Non-zero = no quench
D34	zero or non-zero	Digital input 4. (Inch advance)
D35	zero or non-zero	Digital input 5. (Inch retard)
D36	±65535	Inch trim
D37	±10819	Trim plus software analogue setpoint
D38	±10000.000000	Scaled reference encoder count
D39	±10000.000000	Software analogue loop input
D40	±19999.999999	Ratioed analogue setpoint
D41	±10000	Clamped ratioed analogue setpoint
D42	±819	Scaled trim output
D43	zero or non-zero	Digital input 1. (Halt ramp)
D44	zero or non-zero	Digital input 2. (Phaseloop mode)
D45	zero or non-zero	Digital input 3. (Register mode)
D46	N/A	RESERVED
D47	N/A	RESERVED
D48	zero or non-zero	Digital input 6. (Quench)
D49	±15V	Analogue input 1(Terminal C9)
D50	±15V	Analogue input 2(Terminal C11)
D51	±15V	Analogue output 2(Terminal C5)
D52	±15V	Analogue output 3(Terminal C7)
D53	zero or non-zero	Register loop PI hold Zero = no hold
D54	zero or non-zero	Register loop PI saturated 0 = no saturation Non-zero = saturation
D55	XXXX	Health word
D56	XXXX	Health store
D57	5 to 21.7ms	Cycle true
D58	0 to 1048575	Reference resolution

P No.	Range or value	Function
P1	zero or non-zero	Reference delayed marker source 0 = encoder non-zero = external marker
P2	zero or non-zero	Reference delay clock source 0 = encoder non-zero = external clock
P3	0 to 1048575	Reference marker delay
P4	1 to 1048575	Reference marker resolution
P5	zero or non-zero	Reference marker select 0 = non delayed marker non-zero = delayed marker
P6	N/A	RESERVED
P7	zero or non-zero	Slave delayed marker source 0 = encoder non-zero = external marker
P8	zero or non-zero	Slave delay clock source 0 = encoder non-zero = external clock
P9	0 to 1048575	Slave marker delay
P10	1 to 1048575	Slave marker resolution
P11	zero or non-zero	Slave marker select 0 = non delayed marker non-zero = delayed marker
P12	zero or non-zero	Select reference resolution 0 = resolution equal to P4 non-zero = resolution equal to P10 x P28
P13	1 to 4095	Maximum line speed
P14	0 to 1.500000	Missing mark correction window
P15	zero or non-zero	Missing mark correction enable 0 = no correction Non-zero = correction enabled
P16	0 to 10000	Register loop proportional gain
P17	0 to 10000	Register loop integral gain
P18	zero or non-zero	Register loop PI quench 0 = no quench Non-zero = quench
P19	zero or non-zero	Register loop sign changer 0 = no change Non-zero = inversion
P20	1 to 10000	Register loop +ve clamp
P21	-1 to -10000	Register loop -ve clamp
P22	zero or non-zero	Register loop PI quench select 0 = Digital input 6 Non-zero = P18
P23	zero or non-zero	Encoder source select control Zero = reference encoder non-zero = Speed ref parameter P24
P24	0 to 10000	Speed reference value
P25	0 to 1.000000	Reference speed scaling factor
P26	0 to 1.999999	Ramp time increment
P27	0 to ±1.999999	Reference ratio value

P No.	Range or value	Function
P28	0 to 10000.000000	Feedback resolution scale
P29	zero or non-zero	Serial link ramp reset Zero = no reset Non-zero = reset
P30	zero or non-zero	Serial link ramp halt Zero = no halt Non-zero = halt
P31	zero or non-zero	Ramp reset select control Zero = Digital input 6. (D48) non-zero = Serial link P29
P32	zero or non-zero	Ramp halt select control Zero = Digital input 1. (D43) non-zero = serial link P30
P33	0 to 1.000000	Slave speed scaling factor
P34	zero or non-zero	Slave sign change control Zero = no sign change Non-zero = sign change
P35	N/A	RESERVED
P36	zero or non-zero	Summing junction sign changer Zero = no sign change Non-zero = sign change
P37	0 to 32767	Speedloop proportional gain
P38	0 to 50.000000	Speedloop integral gain
P39	zero or non-zero	Serial link speed PI quench Zero = no quench Non-zero = quench
P40	0 to 32767	Speedloop +ve clamp (0 to 8192 if speedloop)
P41	0 to -32767	Speedloop -ve clamp (0 to - 8192 if speedloop)
P42	zero or non-zero	Speedloop PI quench control Zero = Digital input 6. (D48) non-zero = Serial link P39
P43	zero or non-zero	Speedloop PI hold Zero = no hold Non-zero = hold
P44	0 to 10000	Phaseloop proportional gain
P45	0 to 10000	Phaseloop integral gain
P46	zero or non-zero	Serial link phase PI quench Zero = no quench Non-zero = quench
P47	0 to 8191	Phaseloop +ve clamp
P48	0 to -8191	Phaseloop -ve clamp
P49	zero or non-zero	Phaseloop PI quench control Zero = Digital input 6. (D48) non-zero = Serial link P46
P50	0 to 2048	Inch gain
P51	zero or non-zero	Inch sign Zero = no inversion Non-zero = inversion

P No.	Range or value	Function
P52	zero or non-zero	Serial link inch control Zero = digital input control Non-zero = Serial link control
P53	0 to 10000.000000	Encoder scaling factor
P54	zero or non-zero	Software analogue source control Zero = Scaled reference encoder non-zero = Serial link P55
P55	-10000 to 10000	Speed reference analogue setpoint
P56	zero or non-zero	Software analogue setpoint invert Zero = no inversion Non-zero = inversion
P57	zero or non-zero	Software analogue + trim control Zero = Output, setpoint only Non-zero = setpoint + trim
P58	zero or non-zero	Hardware analogue invert control Zero = no inversion Non-zero = inversion
P59	zero or non-zero	Hardware analogue + trim control Zero = Output, setpoint only Non-zero = setpoint + trim
P60	0 to ±1.999999	Independent analogue ratio
P61	zero or non-zero	SW Analogue ratio select 0 = Digital ratio (D16) non-zero = Independent ratio (P60)
P62	1 to 4096	Zero speed threshold
P63	zero or non-zero	Register trim connected 0 = connected Non-zero = not connected
P64	zero or non-zero	Register enable 0 = disabled (held) non-zero = enabled
P65	zero or non-zero	Reference window enable 0 = disabled Non-zero = enabled
P66	zero or non-zero	Slave window enable 0 = disabled Non-zero = enabled
P67	0 to 3	Digital output 1 selector 0 = Phaseloop PI saturated 1 = Out of synchronisation 2 = Register loop PI saturated 3 = Speedloop PI saturated

P No.	Range or value	Function
P68	0 to 1.000000	Reference mark window
P69	0 to 1.000000	Slave marker window
P70	0 to 1048576.000000	Speedloop PI +ve saturation limit
P71	0 to -1048576.000000	Speedloop PI -ve saturation limit
P72	0 to 1048576.000000	Register loop PI +ve sat limit
P73	0 to -1048576.000000	Register loop PI -ve sat limit
P74	zero or non-zero	Position inch selector 0 = inch output 1 = direct offset parameter (P75)
P75	0 to 204800	Direct position offset
P76	1 to 100	Marker loop PI de-gain factor
P77	Zero or non-zero	Marker loop PI de-gain enable Zero = Auto de-gain disabled non-zero = Auto de-gain enabled
P78	1 to 10000	SW analogue loop filter time constant
P79	Zero or non-zero	HW analogue loop ratio select zero = Digital ratio (D16) non-zero = Independent ratio (P80)
P80	0 to ±1.999999	Independant analogue ratio
P81	0 to ±1000.000000	Speed offset
P82	zero or non-zero	Digin function 0 = terminals B14 and B16 connected to inch block non-zero = terminals B14 and B16 connected to ramp block
P83	0 ± 1.999999	Ramp lower limit
P84	0 ± 1.999999	Ramp upper limit
L1	0 to 2	Loop type variable 0 = Speedloop 1 = Phaseloop 2 = Register loop
L2	zero or non-zero	Looptype source control Zero = Decoded digital inputs Non-zero = Serial link L4
L3	0 to 2	Decoded digital inputs. (As L1)
L4	0 to 2	Serial link looptype. (As L1)

7 HARDWARE DESCRIPTION

7.1 MAIN MICRO - PROCESSOR - 16 BIT

The main processor performs all software control and system functions:

Digital speed, phase and register control loops.

Digital and analog I/O.

Host RS485 serial link.

Operator station RS485 serial link.

Mode selection.

Analog ratio, hardware and software analog loops.

System time control and alarm structure.

Primary LED diagnostics.

7.2 CODE STORAGE MEDIUM

EPROM Capacity 64k Bytes.

7.3 WORKING MEMORY

RAM Capacity 16k Bytes.

7.4 PARAMETER STORAGE MEDIUM

EEPROM Capacity 8k Bytes.

7.5 REFERENCE AND SLAVE GATE ARRAY

The reference and slave gate arrays perform the following tasks:

14 bit PWM analog output.

Multi revolution marker pulse delay unit.

External marker interface.

Fibre optic encoder link diagnostics.

7.6 MULTIPLYING DIGITAL TO ANALOG CONVERTER (D/A)

This device multiplies the reference setpoint by the required ratio factor to produce the hardware analog loop ratioed slave setpoint. The ratioed slave setpoint may be 0 to 1.999999 times the reference setpoint value. The input for the reference setpoint is obtained from analog input 1 (terminal C9). This also goes to the processor for diagnostics. Maximum output is ± 11V.

7.7 DUAL UNIVERSAL ASYNCHRONOUS RECEIVER / TRANSMITTER (DUART)

This device services two serial links and all the digital I/O.

Digital I/O.

Inputs:	Six 24V digital inputs used for the following functions.
Input 1	Run / Halt ramp. Ramp runs if input is low.
Input 2	Phase loop mode. 5720 enters Phaseloop mode if input is high and Input 3 is low.
Input 3	Register mode. 5720 enters Register mode if input is high.
Input 4	Inch advance. The 5720 will inch the slave forward if high.
Input 5	Inch retard. The 5720 will inch the slave backwards if high.
Input 6	Start / Quench. 5720 will Quench if the input is high.
Output1	Selectable for: Phase PI saturation speed PI saturation register PI Saturation out of sync output is inverse of flag
Output2	High if at zero speed.

Host RS485 Serial link

Serial communications to the 5720 are performed using this serial link. The Host serial link allows access to the controller functions as serial messages. The serial link hardware conforms to the international RS485 standard specification, and is of multi-drop format. The serial message transfer format conforms to the Eurotherm BiSynch standard, and as such allows Eurotherm Drives 5720 controllers to be networked together with other instruments within the Eurotherm Group. The slave processor is responsible for the basic protocol handler for message transfer.

Operator Station serial link

This serial link is of the same RS485 EI BiSynch format as the Host serial link. This link is fully compatible with the Host serial link but is intended to interface with the 5721 operator station. The link is driven directly from the processor.

7.8 ALARM SIGNALS

All the alarms listed below are combined in a health word. If an alarm is set the health word will reflect this and the health LED will be off. Alarms are echoed on the 5721 operator station (if enabled).

(a) Self Test

This alarm is triggered if the self test routine fails. The self test routine runs all the time in the background and constantly monitors various functions within the 5720. Many of the points monitored by self test appear as separate alarms.

(b) Analog Outputs

The three analog outputs are monitored and checked against their desired value. If a significant deviation is found, one of the three analog output alarms is set.

(e) 5720 Main Unit EEPROM

This alarm will be raised if a write error of the 5720 EEPROM is detected.

(f) Phaseloop PI Saturation

If the phase loop PI integral value saturates this alarm will trigger.

(g) Speedloop Summing Junction Overflow

This alarm triggers if the summing junction numerical overflow occurs. Data in the speedloop PI integral is then corrupted and accuracy of position cannot be relied upon.

(h) Speedloop PI Saturation

If the speedloop PI integral value saturates this alarm will trigger.

(i) Marker Loop PI Saturation

If the marker loop PI integral value saturates this alarm will trigger.

The 5720's health word is accessible over the serial link as mnemonic EE. In normal (healthy) operation, the health word is 0; an alarm is indicated by a bit becoming set. The word is defined as follows:

Bit no.	Meaning
0	Self test fail
1	Analogue output 1
2	Analogue output 2
3	Reserved
4	Reserved
5	Reserved
6	Reserved
7	EEPROM write fail
8	Looptime overflow
9	Phase loop PI saturated
10	Reserved
11	Speed loop summing junction overflow
12	Speed loop PI saturated
13	Marker loop PI saturated
14	Reserved
15	Reserved

7.9 POWER SUPPLY

This is a separate plug in card. The power supply is powered from 24V dc and generates all the supplies required by the 5720 control card. In addition, the power supply card generates the power on reset and switching for the 24V encoder supply for power on test.

7.10 PRIMARY LED DIAGNOSTICS

Ten LED's are mounted on the 5720 control card. These LED's allow the operational status of the Microtach links and primary health of the 5720 to be monitored. The LED's also provide some information on the running status of the control loops and input signals.

7.11 HARDWARE BLOCK DIAGRAM

The hardware block diagram, figure 7.1, shows the functional layout and content of the 5720 control card. The terminal numbers are shown on the diagram. Exact terminal allocation and function is detailed in section 7.1.4.

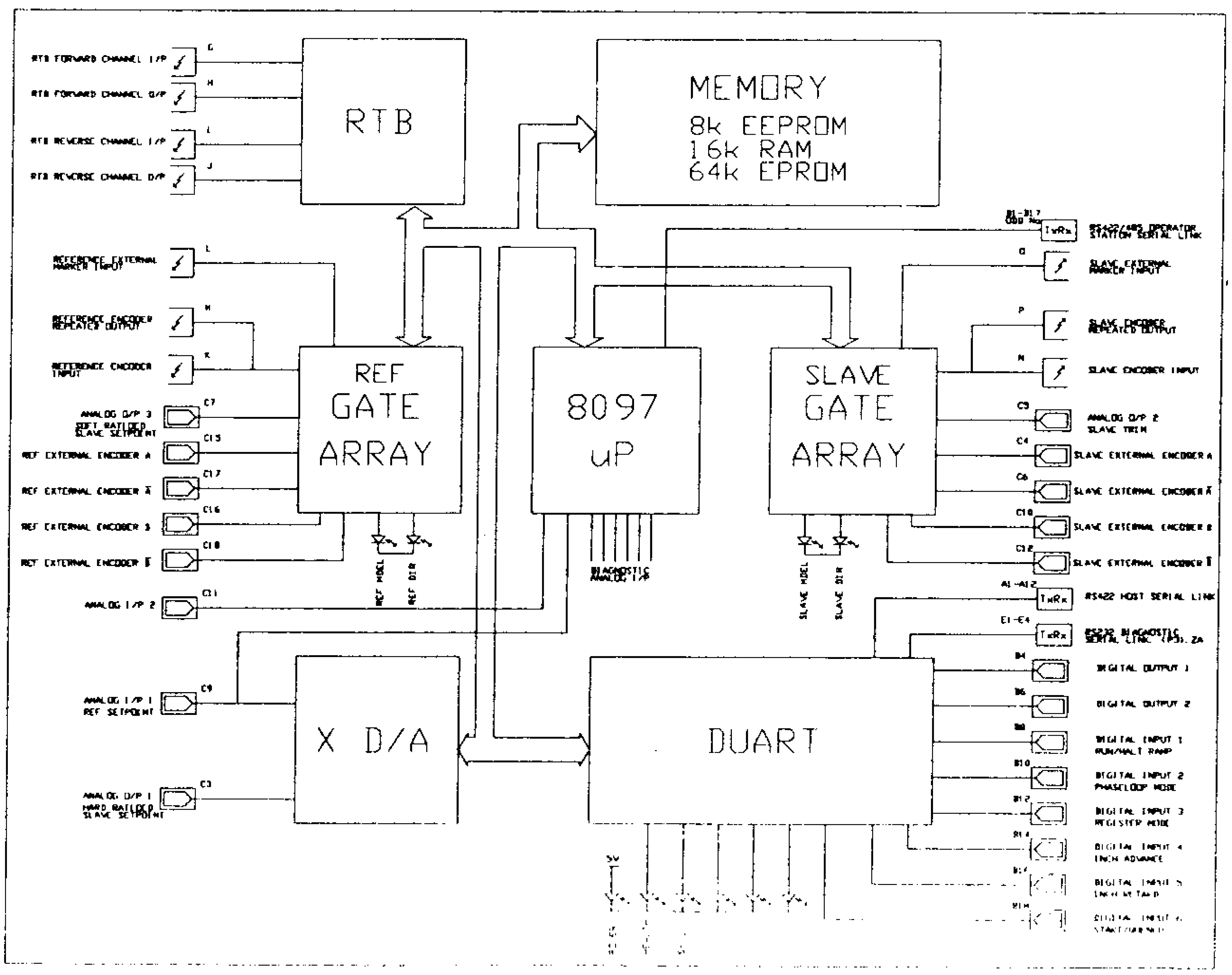


FIG 7.1

7.12 HARDWARE LINKS AND OPTIONS

The following is a list of hardware links and options available on the 5720 control card. All these links are specified in the product code. (Section 3.0).

JUMPER J1	Determines the source of the reference non-delayed marker
Position 1 & 2	Marker is from the reference external marker
Position 2 & 3	Marker is from the reference encoder
JUMPER J2	Defines the reference encoder message rate
Position 1 & 2	Reference encoder message rate is low speed (460.8kHz)
Position 2 & 3	Reference encoder message rate is high speed (921.6kHz)
JUMPER J3	Determines the source of the slave non-delayed marker
Position 3 & 2	Marker is from the slave external marker
Position 1 & 2	Marker is from the slave encoder
JUMPER J4	Defines the slave encoder message rate
Position 2 & 3	Slave encoder message rate is low speed (460.8kHz)
Position 1 & 2	Slave encoder message rate is high speed (921.6kHz)
JUMPER J5	Defines the maximum analog trim strength
Position 1 & 2	Analog trim 10%
Position 2 & 3	Analog trim 100%

7.13 TERMINAL DESCRIPTION

Terminal blocks A, B and C are located along the top of the control board. Terminal block A is a double row 12 way plug-in connector, whilst blocks B and C are 18 way, double row, plug-in connectors. Terminal blocks D, E & F are situated along the bottom of the control board. Blocks D and F are 4 way plug-in type connectors, whilst block E is a telephone style connector. Block Q is a 4 way plug-in type connector and is situated on the angled power card.

The remaining blocks are all fibre optic connectors of the T & B type. Blocks G, I, K, L, N and O are receiver types whilst blocks H, J, M and P are transmitter types.

TERMINAL BLOCK A

A1	0V(Isolated)	Zero volt reference for Host serial link (RS485) only
A2	0V(Isolated)	
A3	RCV+	Serial communication port. (Host link)
A4	RCV+	Receive terminals
A5	RCV-	Balanced line receiver inputs compatible with RS485 signal levels
A6	RCV-	
A7	0V(Isolated)	Zero volt reference for Host serial link (RS485) only.
A8	0V(Isolated)	
A9	XMT+	Serial communication port. (Host link)
A10	XMT+	Transmit terminals
A11	XMT-	Balanced line driver outputs compatible with RS485 signal levels
A12	XMT-	

TERMINAL BLOCK B

B1	0V(Signal ground)	Operator station (5721) power supply.
B3	+24V d.c.	Maximum supply current 1A.
B5	RCV+	Operator station serial port.
B7	RCV-	Receive terminals.
		Balanced line driver outputs compatible with RS485 signal levels.
B9	0V(Isolated)	Operator station serial link 0V only.
B11	XMT+	Operator station serial port.
B13	XMT-	Transmit terminals.
		Balanced line receiver inputs compatible with RS485 signal levels.
B15	0V(Isolated)	Operator station serial link 0V only
B17	0V(Isolated)	Operator station serial link 0V only
B2	0V (Signal ground)	
B4	Digital output 1	Output voltage: +24V d.c.
B6	Digital output 2	Maximum current: 50mA max.
		Output impedance: 47 0hms.
		Not short circuit protected.
B8	Digital input 1	Input voltage: +24V dc.
B10	Digital input 2	Minimum input voltage to operate: +20V dc
B12	Digital input 3	Input current: +5mA.
B14	Digital input 4	Input impedance: 4.7k Ω.
B16	Digital input 5	Sample rate: Once / looptime.
B18	Digital input 6	

TERMINAL BLOCK C

C1	0V (Analog signal ground).	
C3 C5 C7	Analog output 1 Analog output 2 Analog output 3	Bipolar outputs: 0 to ±10V Overdrive: ± 1V Output drive: ± 10V at 5mA Update rate: Once/looptime Resolution (ANOP1): 12 Bits Res (ANOP 2&3): 14 Bit PWM
C9 C11	Analog input 1 Analog input 2	Bipolar inputs: 0 to ± 10V Overload: ± 1V Resolution: 10 Bits Input impedance: 40k Ω Sample rate: Once / looptime
C2 C8 C13 C14	0V (Signal ground) 0V (Signal ground) 0V (Signal ground) 0V (Signal ground)	0V
C15 C17 C16 C18 C4 C6 C10 C12	Not used	

TERMINAL BLOCK D

D1 D2	0V(Power) SW +24V d.c.	Reference encoder switched 24V d.c. power supply. Supply current: 40mA @ 24V d.c.(Max.)
D3 D4	0V(Power) +24V d.c.	Ref external marker input power supply. Supply current: 1A (Max.)

TERMINAL BLOCK E

E1 E2	0V(Signal ground) +24V d.c.	P3 diagnostic port power supply. Supply current: 1A (Max.)
E3	XMT	P3 serial communications port. (Not implemented) Transmit terminal Output compatible with RS232 signal levels.
E4	RCV	P3 serial communications port. (Not implemented) Receive terminal. Input compatible with RS232 signal levels.

TERMINAL BLOCK F

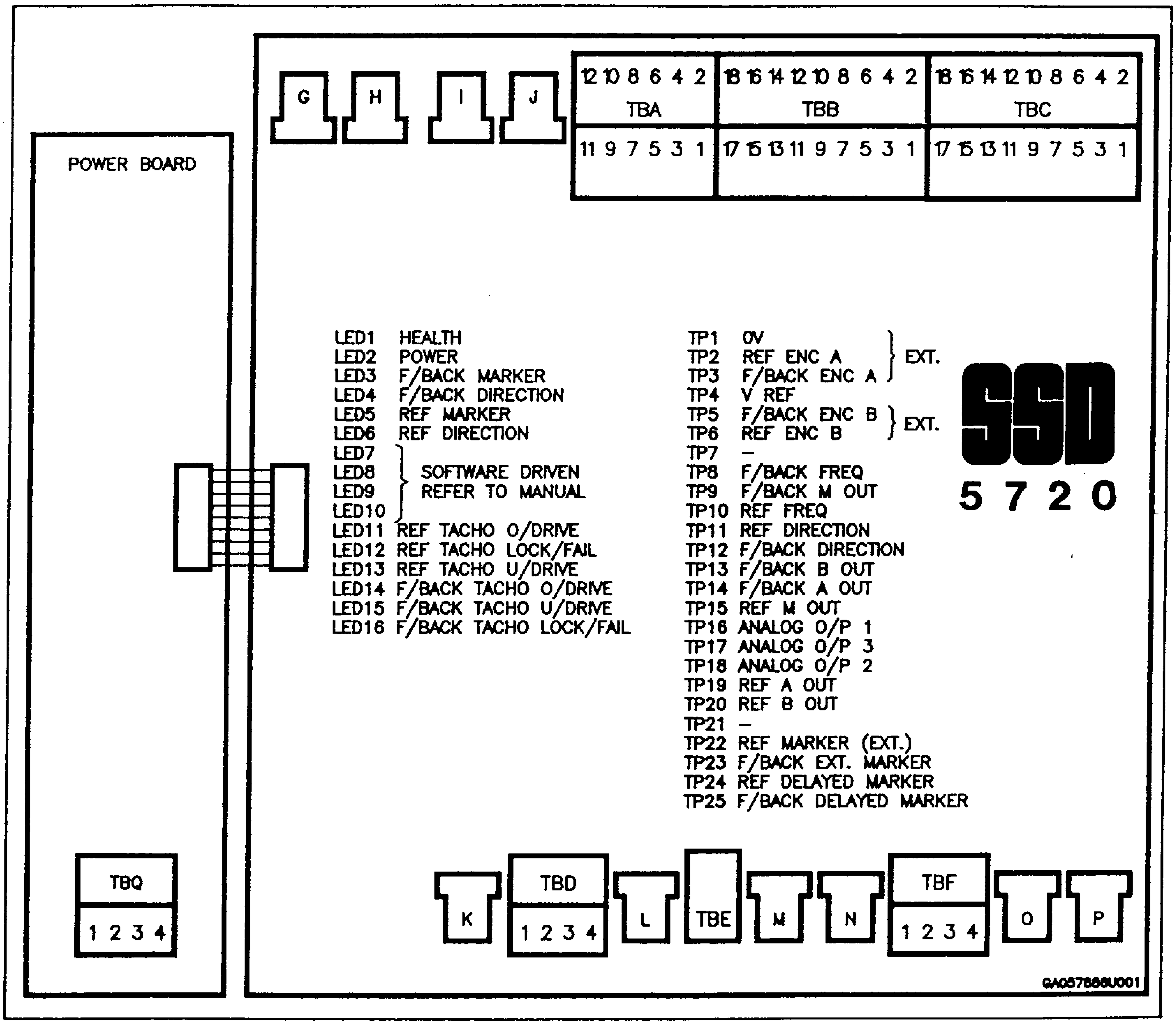
F1 F2	0V(Power) SW +24V d.c.	Slave encoder switched 24V d.c. power supply. Supply current: 40mA @ 24V .d.c.(Max.)
F3 F4	0V(Power) +24V d.c.	Slave external marker input power supply. Supply current: 1A (Max.)

TERMINAL BLOCK Q

Q1	+24V	24V d.c. power supply for 5720.
Q2	0V (power)	To reset connect terminal Q3 to Q4.
Q3	0V(Power)	
Q4	Reset	

FIBRE OPTIC CONNECTORS

G	Receiver	Link forward channel input.
H	Transmitter	Link forward channel output.
I	Receiver	Link reverse channel input.
J	Transmitter	Link reverse channel output.
K	Receiver	Reference encoder input
M	Transmitter	Reference encoder repeated output.
N	Receiver	Slave encoder input.
P	Transmitter	Slave encoder repeated output.
L	Receiver	Reference external marker input.
O	Receiver	Slave external marker input.



8 SETTING UP AND OPERATING INSTRUCTIONS

These notes should be read carefully before attempting to commission a QUADRALOC system. Each step should be followed rigourously as mistakes are easily made but more difficult to find!

8.1 COMMISSIONING NOTES FOR SPEED AND PHASE LOCK

Notes for commissioning speedlock systems:

Before attempting to commission the 5720 the system configuration and values of parameters should be calculated. The basic task of the 5720 is to make the reference speed (D12) and the slave speed (D19) equal. This simple fact should be remembered when calculating scaling factors and ratio values.

The first step of commissioning is to commission the reference and slave drives without QUADRALOC. To do this the system is connected as it would be normally but the QUADRALOC trim (terminal C5) is disconnected from the slave drive. The reference and slave drives are now running purely in analogue with no trim. The reference and slave drives should be run over their speed range and calibrated so that they match each other as closely as possible. This is an important step as differences between the drives will require the trim to work harder and trim saturation limits may be reached. If the slave drive is running backwards change the analogue sign using parameter P58. (Or P56 if the system is configured for tacho following or speed reference).

With the drive running correctly in analogue, the QUADRALOC digital loop can now be checked. Observe variables D12 and D19. They should be approximately the same value but different sign. If their signs are the same, the sign of the slave speed should be changed by using parameter P34. If the signs are correct but the values are very different, check variables D14 & D21, the reference and slave speed inputs. Are they what you calculated them to be? If not, think again. If they are approximately the correct value, remember the drives are running in analogue and no trim has been applied so there could easily be a 1% difference, then check the scaling and ratio values. Assuming the values of D12 and D19 are now correct the next step is to close the loop.

Temporarily quench the trim and apply trim to the slave drive and observe the analogue trim voltage. If no trim voltage appears check the quench and ramp hold functions. If the trim voltage is clamped this will be due to saturation of the speedloop PI integral. This saturation may be due to one of several factors. If it was necessary to invert the analogue voltage setpoint, the trim will also need to be inverted. This may be done by using parameter P36. Another possible source of saturation are the trim inputs D27 and D28. Check that these are set to zero. Lastly, the trim may be saturated if the wrong encoder pre-scaler factors have been used. If the slave drive analogue setpoint is 50% but the reference drive scaling factor is say 0.1 the loop cannot lock as even with full 10% trim the slave drive cannot produce the same encoder frequency as the scaled reference encoder.

If the system appears to be locked but the slave shaft is rotating at the wrong speed, check the calculation of the ratio value. Once the system has been correctly set-up and lock is achieved, fine tuning may take place. After locking the system always check the speedloop error signal (D24) or the analogue trim. If there is a d.c. offset across the speed range, reduce it by modifying the speed calibration of the slave drive. Final checks should be made and tuning of speedloop PI gains may be carried out. The parameter values should then be saved in EEPROM by using the parameter save function of the 5721 operator station. Save all. (Further details may be found in the 5721 operator station manual).

If the system is configured as a tacho/encoder follower, particular care should be taken to check the value of the encoder scaling parameter P53. With 10V applied to the reference drive, full speed, the analogue output on terminal C7 should also be 10V. (Assuming the ratio is set to 1.000000). If the output voltage is incorrect check that D38 is 10000. If it is not, the scaling factor P53 is incorrect. Check D14 and recalculate the scaling factor.

If the system is configured as a speed reference system the correct value of the reference speed (P24) is critical. The simple way of checking P24's value is to run the slave drive at its normal maximum speed with no trim input and observe the scaled feedback value D19. Allowing for reference scaling and ratio the corresponding value of P24 may be calculated. If the system locks but only with a d.c. offset, P24 may be varied to reduce this offset to zero.

Notes for commissioning phaselock systems:

The commissioning of a phaselock system is similar to that of speedlock; the only difference is that there is a second PI to tune. Indeed it may be prudent to initially commission the system as a speedlock system and then change mode to phaselock. It should be remembered that some parameter values may change when changing modes unless those parameters are saved in EEPROM.

8.2 COMMISSIONING NOTES FOR REGISTER LOOPS

The register loop is shown in Figure 6.7. It should be noted that the register loop is an addition to the Phaseloop and the above procedures for commissioning the speed and phase loops should be followed before attempting to commission the register loop. This may be done by configuring the 5720 as a register controller but disabling the register trim by disconnecting it. To do this parameter P63 should be non-zero.

With the reference and slave drives running in phaselock check the arrival of the reference and slave marks. This is most simply done by observing LED's 3 & 5 (or test points 25 and 24). These LED's are situated amongst a group of eight LED's in the bottom left corner of the 5720 control card. LED 3 is the delayed slave mark and is the top left LED, whilst LED 5 is the delayed reference mark and is the top right LED. These LED's change state when a mark occurs. It doesn't matter if both LED's are the same sense or different, but their frequency should be the same. If their frequencies are different check the mark source to see if it is the correct frequency. If the mark source is the correct frequency but the delayed mark is not, check the calculations for delay resolution and try setting the delay values to 1.

Assuming the marks are arriving and being delayed correctly, apply the windows as necessary and check the delayed mark frequency is still correct. If it is not check the delay resolution calculation again. Once correct mark arrival has been established, the ratio value P27 may be tuned. By observing the two delayed marks on an oscilloscope while running as a phaseloop, a slight drifting apart of the marks will be observed. This drifting may be eliminated by careful modification of the ratio value. This step is very important as the phaseloop looks after registration between the mark events.

With the missing mark unit disabled via parameter P14, the register loop trim may now be connected. While at standstill, quench the register PI and set the desired zero speed threshold (P62) and max line speed (P13). Before starting, re-connect the register loop trim using P63. The system may now be run. Check that the register comes into lock at a low speed and then run the system over the whole desired speed range, ensuring that lock is maintained throughout. If the system should lose lock at high speed check the value of max speed (P13). This is easily done by disconnecting the register trim (P63) and running the line at full speed whilst checking D14. P13 should be equal or slightly greater than D14 at full line speed.

Once the loop has locked, the loop may be tuned using the register loop P&I gains P16 and P17. If no problems are encountered the missing mark unit may be enabled if required. If the Missing mark unit repeatedly loses synchronisation, then check that no marks are missing. If both marks are present then widen the missing mark window limits to prevent mis-triggering. The most likely time for the missing mark unit to mis-trigger is during acceleration and deceleration. The accuracy with which the two marks will track each other is dependant upon how accurately the two drives follow each other in analogue only, the tuning of the 5720 PI's and most importantly the mechanics of the system.

Lastly check that registration may be obtained at any point in the cycle by using the delay unit to change the registration point. If lock is lost check the delay resolution and make sure that you are not delaying a channel which has the window feature enabled. Windows and delay are not compatible: if windows are enabled they automatically override the delay feature. Finally check registration over the whole speed range.

8.3 EXAMPLE REGISTRATION APPLICATION

The example shown in figure 8.3 is a downstream printing unit. The reference mark is printed upstream by a CI press and is detected using an electric eye. The electric eye signal is converted into the 5720 fibre optic format using a 5702/6 interface box. Reference web speed is measured using a 5701 Microtach mounted on a reference roll on the web. The position of the downstream print roll is given by a 5701 Microtach mounted directly on the print roll. The mark pulse from this Microtach is again interfaced to the 5720 using a 5702/6. The speed of the print roll is measured using the Microtach attached to the back of the print roll motor. The motor drives the print roll through a gearbox.

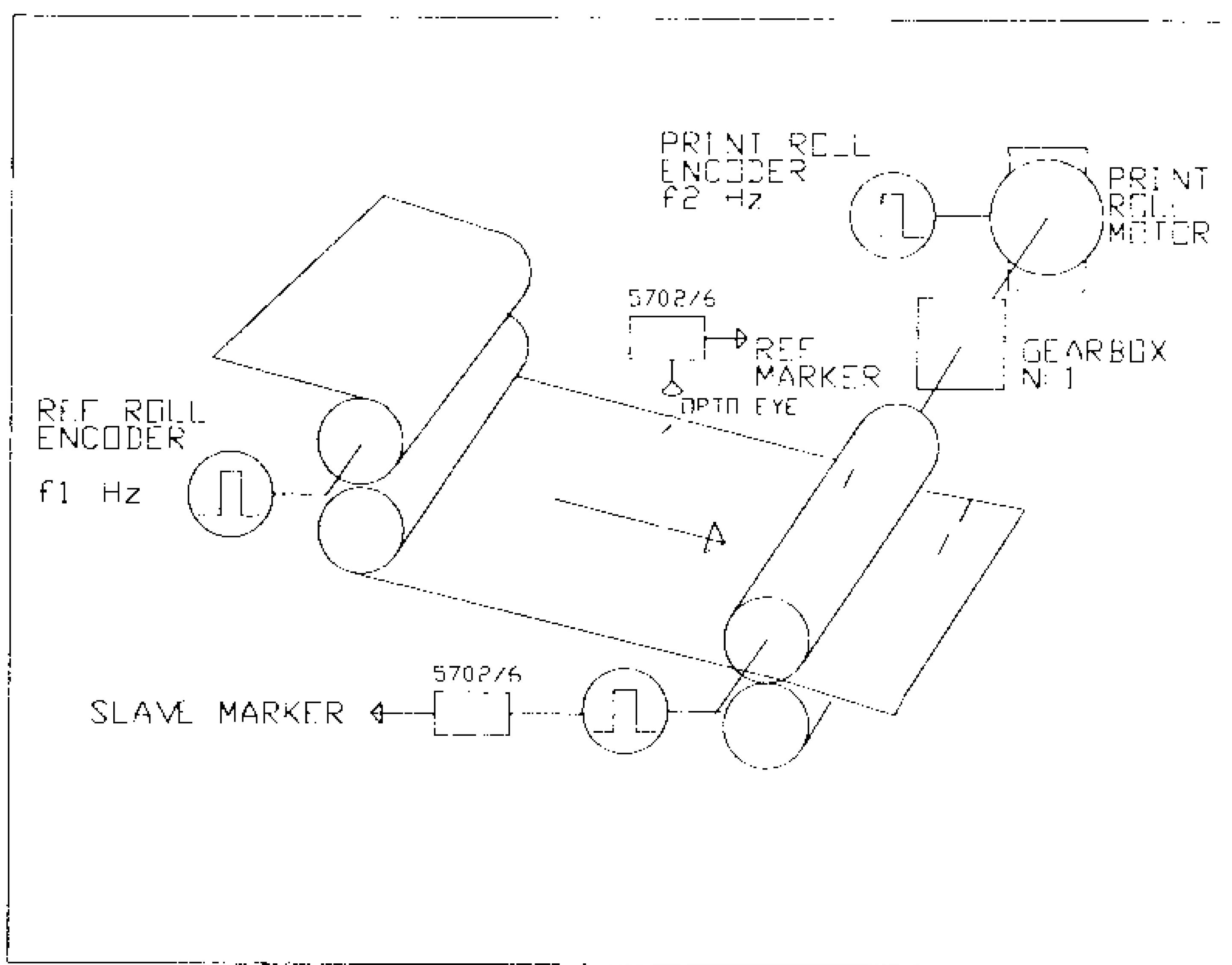


Fig 8.3

All the Microtachs have 1000 pulses/rev and hence 4000 counts/rev. The reference roll has a circumference of 472.4mm and the maximum line speed is 350m/min. For a 1720mm repeat length at a print roll peripheral speed of 350m/min, the motor must run at 744.68RPM. The required print accuracy is ± 1mm. Firstly consider the operation of the phaseloop. At 350m/min the reference roll encoder will produce a count frequency of 49.393kHz. The print roll motor count frequency will be 49.645kHz. The print roll motor must be run at 744.68RPM at full line speed, as the motor is calibrated for 10V = 750RPM then the ratio value must be 0.992907. Thus the ratioed reference encoder count frequency will be 0.992907x49.393kHz = 49.043kHz. Now for the loop to lock the ratioed reference frequency (49.043kHz) and the scaled slave frequency must be equal. As the slave frequency is 49.645kHz this must be multiplied by a scaling factor of 0.987864 to equal the reference frequency. In addition we can calculate the value of Nmax (P13). given a looptime of 10mS then P13 = 49.393kHz x 10mS = 494. Thus:

Ratio(P27) = 0.992907

Reference scaling factor(P25) = 1.000000

Slave scaling factor(P33) = 0.987864

Nmax(P13) = 494

The reference and slave delay resolution figures may be calculated next. The reference roll will rotate 3.7 times / repeat length. Given 4000 counts/rev this gives 14564 counts/ repeat or 8.47 counts/mm. The slave resolution is found from the fact that 350m of web equals 744.68 revolutions of the print roll encoder. Given that the encoder resolution is 4000 counts/rev and the repeat length is 1.72m this gives 14638 counts/repeat or 8.5 counts/mm. These are good values as the accuracy of registration will be typically 10 times the measurement resolution. Thus:

Reference delay resolution(P4) = 14564

Slave delay resolution(P10) = 14638

As we have no reference drive and no reference analogue setpoint the slave drive analogue setpoint must be derived from the reference encoder by using the software analogue loop. We have already calculated Nmax at 350m/min. This value must be converted to represent 10V or a value of 10000. Thus the analogue scaling factor is 10000/494 = 20.245714. Lastly set the zero speed threshold to 5% of maximum line speed. i.e. 5% of 494 = 25. Thus:

Analogue tacho scaling factor(P53) = 20.24571

Zero speed threshold(P62) = 25

8.4 USING THE OPERATOR STATION AS A COMMISSIONING AID

It should be obvious from the above section that attempting to commission a 5720 without a serial link or operator station is virtually impossible. The operator station displays all system variables and parameters with an English title. In addition the operator station will display all error messages. To use the operator station for the commissioning process the user must enter the engineering menu. This special menu allows access to all the 5720's parameters and care should be exercised when operating in this area. To prevent machine operator access to this sensitive menu a password must be entered before access is granted. (It should be noted that no such security exists on the Host RS485 serial link).

In systems which do not require an operator station for normal running, ie: those with a host serial link, the operator station is still useful for commissioning and diagnostics. The operator station may be plugged into or out of a QUADRALOC while power is applied. This allows the user to use one operator station for all his drive section diagnostics and commissioning. Further details about the operator station may be obtained by referring to the operator station manual. (HA058017).

8.5 CONFIGURING THE OPERATOR MENU

The operator menu structure allows the operator to drive the 5720 without knowing how it works. Those parameters and diagnostics to which he needs access are displayed ranged and scaled in engineering units with an English title. An example of this could be delaying the mark. The operator doesn't need to know which mark is being delayed or that their are 8 counts/mm. The operator menu may be configured to display the message MARK DELAY with units of mm, such that the operator may enter the offset directly in mm and not as a count value. Another example would be a local display of line speed. By scaling diagnostic D14 the count value can be converted directly into a display of line speed in m/min.

Their are sixteen possible entries in the operator menu, all may be given a 16 character name, (including spaces), units, and they may be ranged and scaled. The sixteen possible entries are broken down into four groups. The first four entries may be numerical diagnostic (read only), the next four are numerical parameters (read/write), the next are Boolean or switch type diagnostics and the last four are Boolean parameters.

To configure the operator level of the menu enter the engineering level by using the password. Once in the engineering level find "configuration" and press M. This will prompt you with system device. Press M again and by pressing up and down you will be given the choice of 5720, 590 or 570 drive. Select 5720 on the LCD and press enter. You have now selected the 5720 as the system device. Having selected the system device scroll through the display and you will be presented with a list of parameters numbered 1 to 16. 1 to 4 are numeric diagnostics, 5 to 8 are numeric parameters, 9 to 12 are Boolean diagnostics and the last four are Boolean parameters. Configuration information on each of these is detailed below:

PARAMETERS 1 TO 4:

When the display reads PARAMETER X, (where X = 1 to 4), push the M key and the title name will appear. If M is pressed twice a flashing cursor will appear on the lower line. To enter the name use the up and down arrows to cycle through the alphabet and M to select the letter. When the M key is pushed the next letter will flash. If you require a space just push M again. Once the full name has been entered press enter. The display will now prompt you for units. Follow the same procedure as for name but enter spaces first to allow the units to be displayed on the right hand side of the display. Remember that the name will be on the top line of the display and the unit and value will be on the bottom line, so don't make the units name too long.

Having entered the name and units the 5721 will prompt you for the mnemonic. Simply scroll through the list of mnemonics using the up and down arrow keys. Having found the required mnemonic press enter. Next, the display format needs to be entered. This defines the number of integer and decimal places that will be displayed. The display will show the name and units that you have already entered, and a number of i's and d's representing the current selection. To change the display format to, for example, 3 integer digits and one decimal, type 3.1 followed by enter. Lastly at this menu position, use the up and down keys to position the number on the display. The next piece of data required is the formula which will perform the ranging and scaling. Use the arrow keys to scroll through the formulae and the enter key to select it. Having entered the formula the values for the coefficients of A & B must be entered. This is done by pushing M to allow entry of the number, followed by typing in the number on the numeric entry keypad and pushing enter. Having successfully completed the data entry press E and down arrows to enter the next parameter.

PARAMETERS 5 TO 8:

These are read write numeric parameters and are set up in exactly the same way as parameters 1 to 4. In addition to the steps detailed above, two additional questions are asked after entering the required mnemonic. They prompt for lower and upper limits for the parameter. Simply press M and type in the minimum/maximum allowable value for that parameter. These limits prevent the operator entering out of range values.

PARAMETERS 9 TO 12:

These are read only Boolean diagnostics. After entering the name and mnemonic as detailed above, a series of four prompts appear. TEXT FOR VALUE X, (where X = 0 to 3). Each of these is entered in the same way. Press M and enter a text string as you would enter a name. If the D number you are pointing to has only two states such as true/false or zero/non-zero you only need enter text strings for value 0 and value 1.

PARAMETERS 13 TO 16:

These are Boolean read write parameters and are entered in the same way as parameters 9 to 12. In addition to the information required for parameters 9 to 12 you will be prompted to enter the maximum value of the Boolean parameter after entering the mnemonic. Simply push M and type the number of states. The usual number of states is two, i.e. states 0 and 1 so in this case enter 1, but up to four states may be entered.

Having set up all the parameters you require press the down arrow key until you are prompted to enter the display sequence. Press M twice and enter the number of parameters you wish to display. The unit will then display MENU ITEM 1. Using the up and down arrow keys cycle through the list of names you have entered. When the required menu entry is displayed press enter. You will automatically be prompted to select MENU ITEM 2. This is done in the same way as for item 1. Continue until all the items have been selected. To exit the configuration menu keep pressing E until you are in the operator menu. There is no need to save the configuration setup, this is done automatically. However, a "parameter save" will store the information in both the 5720 and the 5721 giving backup security.

9 DIAGNOSTICS

The diagnostics are to aid the user in the identification of faults and error conditions. These diagnostics consist of two different groups. The 'on board' diagnostics are LED's on the printed circuit board which confirm the health of the product and its current operating status. The other diagnostic information is available via the serial link or the operator station. This information gives a more detailed picture of instrument operation and health.

9.1 ON BOARD DIAGNOSTICS

The 'on board' diagnostics consist of sixteen LED's. These LED's show the status of the 5720 without the need to examine the internal software parameters. LED's 1 and 2 are visible through the front panel whilst the other LED's are on the PCB, and are identified by a silk screened legend. The function of the LED's are:

LED1 Health LED. If on the 5720 is healthy.

LED2 Power LED. If on the 24V dc supply is connected.

LED3 FB MDEL. Each occurrence of the slave delayed mark will cause this LED to change state.

LED4 FB DIR. This shows the direction of rotation of the slave shaft. On is rotation in a positive direction.

LED5 REF MDEL. As LED 3 but for the reference mark.

LED6 REF DIR. As LED 4 but for the reference shaft.

LED7 Reserved. (OFF)

LED8 Reserved. (OFF)

LED9 Reserved. (OFF)

LED10 Reserved. (OFF)

LED11 Reserved. (OFF).

LED12 REF LCKF. Reference fibre optic encoder lockfail LED.
If this LED is OFF the decoder for the reference Microtach cannot achieve lock and a message error has been detected.

LED13 REF UD. Reference fibre optic encoder underdrive LED.
If this LED is OFF the reference encoder is not transmitting enough light to be detected by the receiver.

LED14 Reserved. (OFF).

LED15 FB UD. As LED 13 but for the slave fibre optic encoder.

LED16 FB LCKF. As 12 but for the slave fibre optic encoder.

9.2 OPERATOR STATION AND SERIAL LINK DIAGNOSTICS

The operator station (5721) and Host RS485 serial link may be used to look at and modify any Diagnostic or Parameter item in the 5720. Details on how to access these items is given in section 6.7.3. The operator station also automatically announces any fault condition which has caused an alarm. If an alarm condition occurs a message will be displayed. The state of the alarms may be interrogated by entering the engineering menus alarms section. All alarms currently failed will be displayed, in addition the first alarm which caused the failure will be latched in the first alarm flag.

Alarms are announced in a 16 bit hexadecimal health word. Each bit in the word indicates the presence or absence of a specific alarm condition. A bit set in the health word indicates the presence of an alarm. The significance of each bit in the word is as follows :

Bit number	Health word value	Description
0 (L.S.B.)	0001	Self test result. If this bit is set, there is a fault in the 5720, and should be reported to Eurotherm Drives.
1	0002	Analogue output 1 fault. This bit will become set if the 5720 is unable to output a required value. This could be due, for example, to a short circuit.
2	0004	Analogue output 2 fault. This bit will become set if the 5720 is unable to output a required value. This could be due, for example, to a short circuit.
3	0008	Not used.
4	0010	Not used.
5	0020	Not used.
6	0040	Not used.
7	0080	EEPROM failure. When parameters are saved, a write after read test is performed. This bit becomes set if the test fails.
8	0100	Software fault caused by a timer overflow. If this fault occurs it must be reported to Eurotherm Drives.
9	0200	Phase loop saturated. This bit becomes set if the phase loop saturated diagnostic D30 becomes set.
10	0400	Not used.
11	0800	Summing junction overflow. This bit becomes set if the output from the summing junction exceeds the number range.
12	1000	Speed loop saturated. This bit becomes set if the speed loop saturated diagnostic D2 becomes set.
13	2000	Marker loop saturated. This bit becomes set if the marker loop saturated diagnostic D54 becomes set.
14	4000	Not used.
15 (M.S.B.)	8000	Not used.

10 SERVICE INFORMATION

Servicing should only be carried out by qualified service personnel. No attempt should be made to work on the equipment whilst the power is connected.

10.1 ASSOCIATED SYSTEM MODULES

A number of modules are available for use with the 5720, 570 and 590 product ranges. These modules are required for the fibre optic encoder and are powered by 24V d.c, more detail may be obtained from the 5702 product range manual (HA056768).

5702/1 REPEATER. This allows the fibre optic encoder to be used for distances greater than the maximum transmission range of the encoder. Each repeater allows transmission to be increased by the same factor as the maximum transmission distance of the encoder (20 to 40m).

5702/2 TERMINAL RAIL REPEATER. This performs the same function as the 5702/1 but may be mounted on a DIN terminal rail. In addition the module provides single ended decoded A,B and mark signals via a 5V line driver.

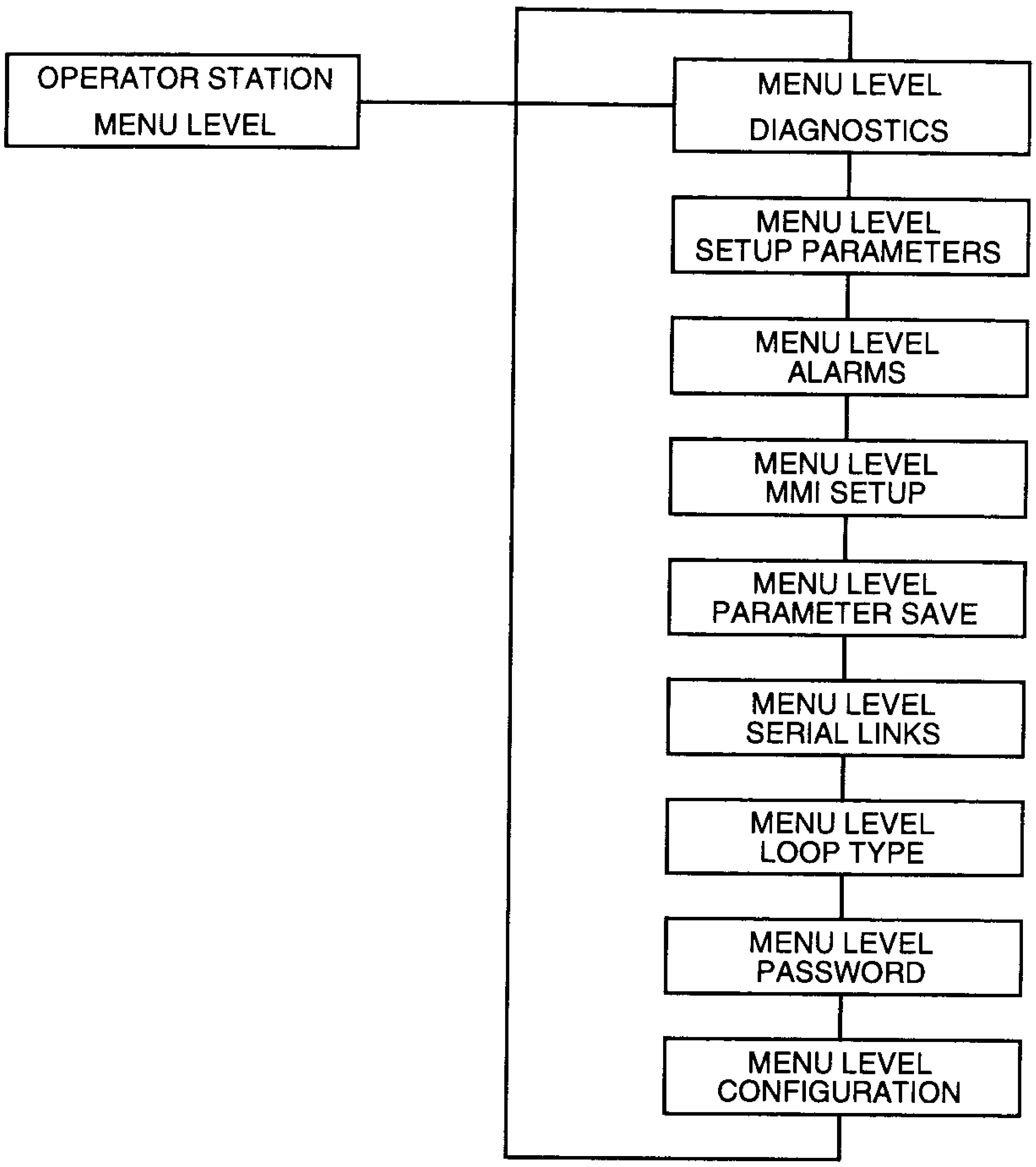
5702/3 ENCODER TO FIBRE CONVERTER. This allows connection of conventional A,B,M incremental encoders to the QUADRALOC system. The encoder may be single ended or differential and may be 5 to 20v. Max encoder rate = 57kHz. The mark must be gated high with A and B high.

5702/6 EXTERNAL MARK INTERFACE. This unit converts external mark sources to fibre optic for use with the 5720 external mark inputs. External sources may be single ended or differential pulses of 5 to 20V. These can include proximity detectors electric eyes and encoders. In addition the 5701 microtach may be connected as the external mark source. This unit must be used whenever external mark sources are connected to the 5720. The 5702/6 may be also used as a repeater for mark signals when the transmission distance exceeds 40 metres.

APPENDIX A

ENGINEER'S MENU STRUCTURE FOR QUADRALOC

LEVEL 1:



APPENDIX B

DIAGNOSTIC POINTS FOR USE WITH QUADRALOC

SUB-MENU NAME	DISPLAY TITLE	VALUE	MNEMONIC	REF	TYPE[1]
MARKER INPUT	OUT OF SYNC	FALSE/ TRUE	f1	D1	1
	NORMALIZED O/P	xxxxx.xxxxxx	m3	D3	4
	ZERO SPEED	TRUE/ FALSE	fc	D5	1
	ENABLE CORRECT'N	NO CORRECTION/ CORRECTION	fa	D6	1
	MISSING MARK O/P	xxxxx.xxxxxx	m7	D7	4
	M LOOP PI INPUT	xxxxx.xxxxxx	m2	D9	4
	M LOOP PI OUTPUT	xxxxx.xxxxxx	m1	D8	4
	MARKER TRIM	xxxxx.xxxxxx	mt	D10	4
	PI QUENCH	UNQUENCHED/ QUENCHED	f5	D11	1
	PI HOLD	OFF/ON	fb	D53	1
	M LOOP PI SAT	UNSATURATED/ SATURATED	fe	D54	1
	REF RESOLUTION[4]	xxxxxx	md	D58	4
REF INPUT	RATIOED REF	xxxx	sr	D12	4
	MASTER SPEED	xxxxx	s1	D13	2
	UNSCALED REF IP	xxxxx	s2	D14	2
	NORMALIZED REF	xxxx	sn	D15	4[2]
	RAMPED RATIO	x.xxxxxx	sg	D16	4
	RAMP QUENCH	UNQUENCHED/ QUENCHED	f6	D17	1
	RAMP HALT	RUN/HALT	f7	D18	1
FEEDBACK INPUT	SIGNED FEEDBACK	xxxx	ss	D19	4[2]
	SLAVE SPEED	xxxxx	s3	D20	2
	UNSCALED FB IP	xxxxx	s4	D21	2
	NORMALIZED FB	xxxx	sf	D22	4[2]
SPEED LOOP P.I.	SUMMING JCT OV	NO OVERFLOW/ OVERFLOW	f3	D23	1
	SPEED LOOP ERROR	xxxxxxxx.xxxxxx	se	D24	4
	S LOOP PI OUTPUT	xxxxxxxx.xxxxxx	so	D25	4
	SPEED LOOP TRIM	xxxxx	st	D26	2
	SPEED TRIM 1	xxxxx.xxxxxx	t1	D27	4
	SPEED TRIM 2	xxxxx.xxxxxx	t2	D28	4
	PI QUENCH	UNQUENCHED/ QUENCHED	f8	D29	1
	S LOOP PI SAT	UNSATURATED/ SATURATED	fd	D2	1

PHASE P.I.	P LOOP PI SAT	UNSATURATED/ SATURATED	f4	D30	1
	P LOOP PI OUTPUT	xxxxx	po	D31	2
	PHASE LOOP TRIM	xxxxx	pt	D32	2
	PI QUENCH	QUENCHED/ UNQUENCHED	f9	D33	1
INCH	INCH ADVANCE	FALSE/ TRUE	ia	D34	1
	INCH RETARD	FALSE/ TRUE	ir	D35	1
	INCH TRIM	xxxxx	it	D36	4[2]
SW ANALOG LOOP	ANALOG OUTPUT	xxxxx	ao	D37	2
	SUMMED REFERENCE	xxxxx	m6	D4	3
	SCALED INPUT	xxxxx	ay	D38	2
	MASTER SETPOINT	xxxxx	as	D39	2
	RATIOED REF	xxxxx	ar	D40	2
	CLAMP OUTPUT	xxxxx	ac	D41	2
	LOOP TRIM	xxxxx	at	D42	2
DIGITAL INPUTS	INPUT 1 TBB8	OFF/ ON	d1	D43	1
	INPUT 2 TBB10	OFF/ ON	d2	D44	1
	INPUT 3 TBB12	OFF/ ON	d3	D45	1
	INPUT 4 TBB14	OFF/ ON	d4	D46	1
	INPUT 5 TBB16	OFF/ ON	d5	D47	1
	INPUT 6 TBB18	OFF/ ON	d6	D48	1
ANALOG I/O	INPUT 1 TBC9	xx.xx VOLTS	a1	D49	2
	INPUT 2 TBC11	xx.xx VOLTS	a2	D50	2
	OUTPUT 2 TBC5	xx.xx VOLTS	o1	D51	2
	OUTPUT 3 TBC7	xx.xx VOLTS	o2	D52	2
SYSTEM VALUES	HEALTH WORD	xxxx	he	D55	1
	HEALTH STORE	xxxx	hs	D56	1
	CYCLE TIME	5 - 21.7ms	ct	D57	2

PARAMETRIC POINTS FOR USE WITH QUADRALOC

SUB-MENU NAME	DISPLAY TITLE	VALUE	RANGE	MNEMONIC	REF	TYPE[1]
MARKER LOOP: REFERENCE INPUT	SELECT REF INPUT	ENCODER/ EXTERNAL		x6	P1	1
	SELECT REF CLOCK	ENCODER/ EXTERNAL		x7	P2	1
	REFERENCE DELAY	xxxxxxx	0 to 1048575	m4	P3	4[2]
	REF RESOLUTION	xxxxxxx	1 to 1048575	m8	P4	4[2]
	REF MARK SELECT	REFERENCE MARKER/ DELAYED REF MARK		xa	P5	1
	REF WINDOW	DISABLE/ ENABLE		xg	P65	1
	REF MARK WINDOW	x.xxxxxx	0 to 1	mu	P68	4
	SELECT REF RES[4]	DIRECT/ SCALED FB RES		ml	P12	1
	FB RES SCALE[4]	xxxxx.xxxxxx	0 TO 10000.000000	ms	P28	4
FEEDBACK INPUT	SELECT FB INPUT	ENCODER/ EXTERNAL		x8	P7	1
	SELECT FB CLOCK	ENCODER/ EXTERNAL		x9	P8	1
	FEEDBACK DELAY	xxxxxxx	0 to 1048575	m5	P9	4[2]
	FB RESOLUTION	xxxxxxx	1 to 1048575	m9	P10	4[2]
	FB MARK SELECT	FEEDBACK MARKER/ DELAYED FB MARK		xb	P11	1
	FEEDBACK WINDOW	DISABLE/ ENABLE		xh	P66	1
	FB MARK WINDOW	x.xxxxxx	0 to 1	mv	P69	4
P.I.	MAX SPEED	xxxx	1 to 4095	mb	P13	3
	CORRECTION RATIO	x.xxxxxx	0 to 1.5	mc	P14	4
	ENABLE CORRECT'N	NO CORRECTION/ CORRECTION		w3	P15	1
	M LOOP PROP GAIN	xxxxxxxx.xxxxxx	0 to 10000	mp	P16	4
	M LOOP INT GAIN	xxxxxxxx.xxxxxx	0 to 10000	mi	P17	4
	M LOOP PI QUENCH	UNQUENCHED/ QUENCHED		w4	P18	1
	M LOOP SIGN	NORMAL/ INVERT		wc	P19	1

	+ve M LOOP CLAMP	xxxxx	1 to 10000	m+	P20	4[2]
	-ve M LOOP CLAMP	xxxxx	-1 to -10000	m-	P21	4[2]
	QUENCH CONTROL	DIGITAL INPUT/ SERIAL INPUT		x1	P22	1
	ZERO SPD THRESH	xxxx	1 to 4096	ma	P62	3
	REGISTER ENABLE	DISABLED/ ENABLED		wl	P64	1
	DISCONNECT TRIM	CONNECTED/ DISCONNECTED		xf	P63	1
	M LOOP +ve ERROR	xxxxxxx.xxxxxx	0 to 1048576	mw	P72	4
	M LOOP -ve ERROR	xxxxxxx.xxxxx	0 to -1048576	mx	P73	4
	DE-GAIN FACTOR	xxxx	1 to 1000	w1	P76	3
	AUTO DE-GAIN	ENABLED/ DISABLED		my	P77	1
REF INPUT	RATIO	x.xxxxxx	0 to ±1.999999	sb	P27	4
	SELECT REF INPUT	MASTER SPEED/ SPEED REFERENCE		xc	P23	1
	SPEED REFERENCE	xxxxx	0 to 10000	s5	P24	3
	REF SCALE FACTOR	x.xxxxxx	0 to 1.000000	sm	P25	4
	RAMP GRADIENT	x.xxxxxx	0 to 1.999999	sa	P26	4
	RAMP QUENCH	UNQUENCHED/ QUENCHED		wg	P29	1
	RAMP HALT	RUN/ HALT		wh	P30	1
	RAMP QUENCH CNTL	DIGITAL INPUTS/ SERIAL INPUTS		x2	P31	1
	RAMP HALT CNTL	DIGITAL INPUTS/ SERIAL INPUTS		x3	P32	1
	DIGIN FUNCTION[4]	INCH/ RAMP RATIO		re	P82	1
	RAMP LOWER LIMIT[4]	x.xxxxxx	0 to ±1.999999	rl	P83	4
	RAMP UPPER LIMIT[4]	x.xxxxxx	0 to ±1.999999	ru	P84	4
	INVERT RATIO SRC	SERIAL/DIGITAL		xk	P85	1
	INVERT RATIO	FALSE/TRUE		xl	P86	1
FEEDBACK INPUT	FB SCALE FACTOR	x.xxxxxx	0 to 1.000000	sc	P33	4
	FEEDBACK SIGN	NORMAL/ INVERT		w6	P34	1
SPEED LOOP P.I.	ERROR SIGN	NORMAL/ INVERT		w7	P36	1
	S LOOP PROP GAIN	xxxxxxxx.xxxxxx	0 to 32767	sp	P37	4
	S LOOP INT GAIN	xxxxxxxx.xxxxxx	0 to 50	si	P38	4
	S LOOP PI QUENCH	UNQUENCHED/ QUENCHED		w8	P39	1
	+ve S LOOP CLAMP	xxxxx	0 to 32767	s+	P40	3
	-ve S LOOP CLAMP	xxxxx	0 to -32767	s-	P41	3[3]
	QUENCH CONTROL	DIGITAL INPUTS/ SERIAL INPUTS		x4	P42	1

	PI HOLD	RUN/HOLD		wj	P43	1
	S LOOP +ve ERROR	xxxxxxx.xxxxxx	0 to 1048576	su	P70	4
	S LOOP -ve ERROR	xxxxxxx.xxxxxx	0 to -1048576	sv	P71	4
	SPEED OFFSET	xxxx.xxxxxx	0 ± 1000	sz	P81	4
PHASE P.I.	P LOOP PROP GAIN	xxxxx	0 to 10000	pp	P44	3
	P LOOP INT GAIN	xxxxx	0 to 10000	pi	P45	3
	P LOOP PI QUENCH	UNQUENCHED/ QUENCHED		w9	P46	1
	+ve P LOOP CLAMP	xxxxx	0 to 8191	p+	P47	2
	-ve P LOOP CLAMP	xxxxx	0 to -8191	p-	P48	2
	QUENCH CONTROL	DIGITAL INPUTS/ SERIAL INPUTS		x5	P49	1
INCH	INCH GAIN	xxxxx	0 to 2048	ii	P50	3
	INCH SIGN	NORMAL/ INVERT		wf	P51	1
	SERIAL LINK CNTL	NO INCH/ INCH		wk	P52	1
	POS OFFSET CNTL	INCH/DIRECT		xi	P74	1
	POS OFF R GRAD	xxxx	0 to 2048	ig	P6	3
	POSITION OFFSET	xxxxxx	0 to 204800	io	P75	4
SW ANALOG LOOP	TACHO SCALER	xxxxx.xxxxxx	0 to 10000	am	P53	4
	SELECT REF INPUT	MASTER SPEED/ SPEED REFERENCE		xc	P54	1
	ANALOG REFERENCE	xxxxx	-10000 to 10000	ax	P55	2
	ANALOG SIGN	NORMAL/ INVERT		wb	P56	1
	ADD TRIM	OFF/ ON		xd	P57	1
	RATIO SELECT	DIGITAL RATIO/ ANALOG RATIO		rs	P61	1
	ANALOG RATIO	x.xxxxxx	0 to ±1.999999	ra	P60	4
	FILTER CONSTANT	xxxxx	1 to 10000	cf	P78	3
HW ANALOG LOOP	ANALOG SIGN	NORMAL/ INVERT		wb	P58	1
	ADD TRIM	OFF/ON		xe	P59	1
	RATIO SELECT	DIGITAL RATIO/ ANALOG RATIO		hr	P79	1
	ANALOG RATIO	x.xxxxxx	0 to ±1.999999	rb	P80	4
DIG OP 1 SELECT	DIG OP 1 SELECT	PHASE PI SAT/ OUT OF SYNC/ MARKER PI SAT/ SPEED PI SAT		d9	P67	6

LOOP TYPE CONTROLS FOR USE WITH QUADRALOC

SUB-MENU NAME	DISPLAY TITLE	VALUE	MNEMONIC	REF	TYPE[1]
LOOP TYPE	ACTUAL	SPEED LOOP/ PHASE LOOP/ MARKER LOOP	lt	L1	5
	CONTROL SOURCE	DIGITAL INPUTS/ SERIAL INPUTS	wi	L2	1
	DIGITAL INPUTS	SPEED LOOP/ PHASE LOOP/ MARKER LOOP	ld	L3	5
	SERIAL INPUTS	SPEED LOOP/ PHASE LOOP/ MARKER LOOP	ls	L4	5

Note 1
The type column indicates the data type of the variable. All serial link messages conform to the Eurotherm ASCII Bisynch protocol, format 23 (variable length hexadecimal). The type column indicates the number of data bytes in the data field from the following table.

Type 1 — Two value (binary) type. The data field consists of a ASCII single character, with value 0 or 1. In this appendix, the MMI display for the zero value is shown first.

Type 2 — Signed word type. The data field consists of four characters, each an ASCII coded hexadecimal digit. They form a 2's complement word; the highest order nibble is transmitted first.

Type 3 — Unsigned word type. The data field consists of four characters, each an ASCII coded hexadecimal digit. They form an unsigned 16 bit word; the highest order nibble is transmitted first.

Type 4 — Long type. The data field consists of 16 characters, each an ASCII coded hexadecimal number. The first 8 characters form the 4 byte magnitude plus sign integer part of the number. The sign is the most significant bit of the most significant of the 4 bytes. The last 8 characters form an 4 byte decimal part. The decimal part can take the value 00000000_{16} to $000F423F_{16}$, representing 0.000000_{10} to 0.999999_{10}.

Type 5 — Three state type. It is used for loop type variables. The data field consists of two characters. The first ASCII character is 0; the second character may take the following values:

Value	Loop type
0	Speed loop
1	Phase loop
2	Marker loop

Type 6 — Four state type. It is used to define the signal source for digital output 1. The data field consists of two characters. The first character is 0; the second character may take the following values:

Value	Source
0	PHASE PI SAT
1	OUT OF SYNC
2	MARKER PI SAT
3	SPEED PI SAT

Note 2
Only the integer part of the value is significant. The decimal part should be ignored when reading the parameter, and set to 0 when writing to it.

Note 3
This is an unsigned number; the 5720 converts to negative internally.

Note 4
These diagnostics and parameters were introduced at software version 2.12. If they are to be accessed on a 5721, this should have software version 3.4 or later.

APPENDIX C

SUB-MENU NAME	DISPLAY TITLE	REF	DEFAULT VALUE	USER VALUE
MARKER LOOP: REFERENCE INPUT	SELECT REF INPUT	P1	ENCODER(00H)	
	SELECT REF CLOCK	P2	ENCODER(00H)	
	REFERENCE DELAY	P3	1	
	REF RESOLUTION	P4	4000	
	REF MARK SELECT	P5	DELAYED REF MARK (7FH)	
	REF WINDOW	P65	DISABLE(00H)	
	REF MARK WINDOW	P66	0.999500	
	SELECT REF RES	P12	DIRECT	
	FB RES SCALE	P28	0	
FEEDBACK INPUT	SELECT FB INPUT	P7	ENCODER(00H)	
	SELECT FB CLOCK	P8	ENCODER(00H)	
	FEEDBACK DELAY	P9	1	
	FB RESOLUTION	P10	4000	
	FB MARK SELECT	P11	DELAYED FB MARK(7FH)	
	FEEDBACK WINDOW	P66	DISABLE(00H)	
	FB MARK WINDOW	P69	0.999500	
P.I.	MAX SPEED	P13	2000	
	CORRECTION RATIO	P14	0.000001	
	ENABLE CORRECT'N	P15	NO CORRECTION(00H)	
	M LOOP PROP GAIN	P16	350.000000	
	M LOOP INT GAIN	P17	3.000000	
	M LOOP PI QUENCH	P18	UNQUENCHED(00H)	
	M LOOP SIGN	P19	NORMAL(00H)	
	+ve M LOOP CLAMP	P20	10000.000000	
	-ve M LOOP CLAMP	P21	-10000.000000	
	QUENCH CONTROL	P22	DIGITAL INPUT(00H)	
	ZERO SPD THRESH	P62	1	
	REGISTER ENABLE	P64	ENABLED(7FH)	
	DISCONNECT TRIM	P63	CONNECTED(00H)	
	M LOOP +ve ERROR	P72	1048575	
	M LOOP -ve ERROR	P73	-1048575	
	DE-GAIN FACTOR	P76	1	
	AUTO DE-GAIN	P77	DISABLED(00H)	

REF INPUT	RATIO	P27	1.000000	
	SELECT REF INPUT	P23	MASTER SPEED(00H)	
	SPEED REFERENCE	P24	2000	
	REF SCALE FACTOR	P25	1.000000	
	RAMP GRADIENT	P26	1.000000	
	RAMP QUENCH	P29	UNQUENCHED(00H)	
	RAMP HALT	P30	RUN(00H)	
	RAMP QUENCH CNTL	P31	DIGITAL INPUTS(00H)	
	RAMP HALT CNTL	P32	DIGITAL INPUTS(00H)	
	DIGIN FUNCTION	P82	INCH	
	RAMP LOWER LIMIT	P83	-1.999999	
	RAMP UPPER LIMIT	P84	+1.999999	
	INVERT RATIO SRC	P85	SERIAL INPUTS(00H)	
	INVERT RATIO	P86	FALSE	
FEEDBACK INPUT	FB SCALE FACTOR	P33	1.000000	
	FEEDBACK SIGN	P34	NORMAL(00H)	
SPEED LOOP P.I.	ERROR SIGN	P36	NORMAL(00H)	
	S LOOP PROP GAIN	P37	50	
	S LOOP INT GAIN	P38	12	
	S LOOP PI QUENCH	P39	UNQUENCHED(00H)	
	+ve S LOOP CLAMP	P40	32767	
	-ve S LOOP CLAMP	P41	-32767	
	QUENCH CONTROL	P42	DIGITAL INPUTS(00H)	
	PI HOLD	P43	RUN(00H)	
	S LOOP +ve ERROR	P70	1048575	
	S LOOP -ve ERROR	P71	-1048575	
	SPEED OFFSET	P81	0	
PHASE P.I.	P LOOP PROP GAIN	P44	175	
	P LOOP INT GAIN	P45	50	
	P LOOP PI QUENCH	P46	UNQUENCHED(00H)	
	+ve P LOOP CLAMP	P47	8191	
	-ve P LOOP CLAMP	P48	-8191	
	QUENCH CONTROL	P49	DIGITAL INPUTS(00H)	
INCH	INCH GAIN	P50	1	
	INCH SIGN	P51	NORMAL(00H)	
	SERIAL LINK CNTL	P52	NO INCH(00H)	
	POS OFFSET CNTL	P74	INCH(00H)	
	POS OFF R GRAD	P6	2048	
	POSITION OFFSET	P75	0	
SW ANALOG LOOP	TACHO SCALER	P53	5.000000	
	SELECT REF INPUT	P54	MASTER SPEED(00H)	
	ANALOG REFERENCE	P55	1000	
	ANALOG SIGN	P56	INVERT (7FH)	
	ADD TRIM	P57	OFF(00H)	
	RATIO SELECT	P61	DIGITAL RATIO(00H)	
	ANALOG RATIO	P60	1.000000	
	FILTER CONSTANT	P78	1	

HW ANALOG LOOP	ANALOG SIGN ADD TRIM RATIO SELECT ANALOG RATIO	P58 P59 P79 P80	INVERT (7FH) OFF(00H) DIGITAL RATIO(00H) 1.000000	
DIG OP 1 SELECT	DIG OP 1 SELECT	P67	SPEED PI SAT(03H)	

ISS.	MODIFICATION	CP.NO.	DATE	APPROVAL
1	Initial Issue	3378	26.9.90	DEB
2	This version of the manual applies to Issue 2 pcb's onwards. Add to section 2 Looptime - 16ms (Version 2.3). Change Product code to 26 digits (section 3). Changes to Section 7.13. J2, J1. Swap position 1 and 2 - 2 and 3. Remove J8, J9, J10 and J11. Change J6 to SW2 and J7 to SW3 and add position 3. (Position 1 0-20m, position 2 20-40m and position 40-60m).	3384	26.11.90	DEB
3	Re-draw of Block Diagrams.	6304	19.02.91	GDR
4	Add to section 4 method of terminating fibre optic cables	7659	28.08.92	AFL
5	Add to section 6 and block diagrams speed offset, software loop filter. Many detail corrections.	7243	16.10.92	AFL
6	Update Manual to include changes introduced at Software version 2.12. Replaced SSD with Eurotherm Drives.	8042	30.11.92	AFL
7	Penultimate para. of 6.6.1 re-written. New features introduced at Software version 2.15 described in 6.1.3. and parameters P85, P86 added to appendix B. Health word described in 9.2. Fig. 6.1 modified. New parameters added to appendices B and C.	10701	06.03.96	[signature]

FIRST USED ON	MODIFICATION RECORD 5720 Quadraloc Drive Synchronisation Unit
EUROTHERM DRIVES	DRAWING NUMBER ZZ058183C — SHT. 1 of 1 SHTS

ISS.	MODIFICATION	CP.NO.	DATE	APPROVAL
	5720 Manual HA058183 Sheet 1 filed in Drawing Office			
8	Page 7-4 changed:- B5 XMT+ to B5 RCV+, B7 XMT- Transmit terminals to B7 RCV- Receive terminals. B11 RCV+ to B11 XMT+ B13 RCV- Receive terminals to B13 XMT- Transmit	11064	15.05.97	AFL.

FIRST USED ON	MODIFICATION RECORD 5720 Quadraloc Drive Synchronisation Unit	
EUROTHERM DRIVES	DRAWING NUMBER ZZ058183C	SHT. 2 of 2 SHTS